

32-bit RISC Microcontroller

CMOS

FR20 Series MB91103

MB91103

■ DESCRIPTION

The MB91103 is a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR20 Series) core with abundant I/O resources and bus control functions optimized for high-performance/high-speed CPU processing for embedded controller applications. To support the vast memory space accessed by the 32-bit CPU, the MB91103 normally operates in the external bus access mode and executes instructions on the internal 1 KB cache memory for enhanced performance.

The MB91103 is optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

■ FEATURES

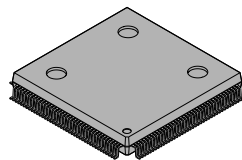
FR20CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency: 25 MHz
- General purpose registers: 32-bit × 16
- 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications
- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages
- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots: Reduced overhead time in branch executions
- Internal multiplier/Supported at instruction level
 - Signed 32-bit multiplication: 5 cycles
 - Signed 16-bit multiplication: 3 cycles
- Interrupt (push PC and PS): 6 cycles, 16 priority levels

(Continued)

■ PACKAGE

160-pin Plastic QFP



(FPT-160P-M03)

MB91103 Series

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Bus interface

- 24-bit address bus (16 MB memory space)
- 32-bit/16-bit/8-bit data bus
- Basic external bus cycle: 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 K bytes: 6
- Interface supported for various memory technologies
 - Time sharing input/output of data/address (area 1)
 - DRAM interface (area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
- Parity check function: Generates parity error interrupt
- Unused data/address pins can be configured as input/output ports
- Little endian mode supported (Select 1 area from area 1 to 5)

DRAM interface

- 2 banks independent control (area 4 and 5)
- Normal mode/high speed page mode
- Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high speed page mode
- Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
 - CBR refresh (interval time configurable by 6-bit timer)
 - Self-refresh mode
- Supports 8-bit/9-bit/10-bit/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

Cache memory

- 1 KB instruction cache memory
- 2 way set associative
- 32 blocks/way, 4 entries (4 words)/block

DMAC (DMA Controller)

- 5 channels
- External to external 2.5 access cycle/transfer (when 2 clock cycles = 1 access cycle)
- Internal to external 1.5 access cycle/transfer (when 2 clock cycles = 1 access cycle)
- Address registers (inc, dec and reload executable), 32-bit \times 2, 16-bit \times 6
- Transfer count register (reload executable), 16-bit \times 2, 8-bit \times 3
- Transfer incident/external pins/internal resource interrupt requests/software interrupts
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer/cycle steal transfer (for ch. 0 and ch.1 only)
- Transfer data length: 8-bit/6-bit/32-bit selective
- Command chain operation possible
- NMI/interrupt request enables temporary stop operation

UART

- 2 independent channels
- Full-duplex double buffer
- Data length: 7-bit to 9-bit (non-parity), 6-bit to 8-bit (parity)
- Asynchronous (start-stop system), CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer operating as a proprietary baud rate generator: Generates any given baud rate
- Use external clock can be used as a transfer clock
- Error detection: Parity, frame, overrun

(Continued)

Extended I/O serial interface

- Inputs/outputs 8-bit data in serial format
- LSB first/MSB first selective
- Shift clock internal generation/external input selective

A/D converter (successive approximation type)

- 10-bit resolution, 8 channels
- Successive approximation type: Conversion time of 5.6 μ s at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion selective
- Start: Software/external trigger/internal timer selective

Reload timer

- 16-bit timer: 2 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective
- Pin input: Event counter input/gate function
- Square wave output

Up/down counter

- 16-bit timer: 2 channels
- Timer mode/up/down counter mode/phase shift count mode
- Pin input activates counter clear/gate function

Other interval timers

- 16-bit timer: 2 channels (U-TIMER), 1 channel (free run for ICU/OCU)
- Watch-dog timer: 1 channel

Input capture/output compare

- Capture: 4 channels, compare: 8 channels
- Count can be cleared on compare match
- 16-bit unified free-run timer embedded

Bit search module

- First bit transition "1"/"0" from MSB can be detected in 1 cycle

Interrupt controller

- External interrupt input: Non-maskable interrupt ($\overline{\text{NMI}}$), normal interrupt $\times 8$ (INT0 to INT7)
- Internal interrupt incident: Parity error, UART, DMAC, A/D, reload timer, up/down counter, capture/compare, baud rate timer, extended serial I/O, free-run timer and delayed interrupt
- Priority levels of interrupts are programmable in 16 steps (except for non-maskable interrupt)

Others

- Reset cause: Power-on reset/watch-dog timer/software reset/external reset
- Low power consumption mode
Sleep mode/stop mode
- Clock gear function
Operating clocks for CPU and peripherals are independently selective
Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16)
- Package
QFP-160
- CMOS technology (0.65 μ m), operating voltage 5.0 V $\pm 10\%$

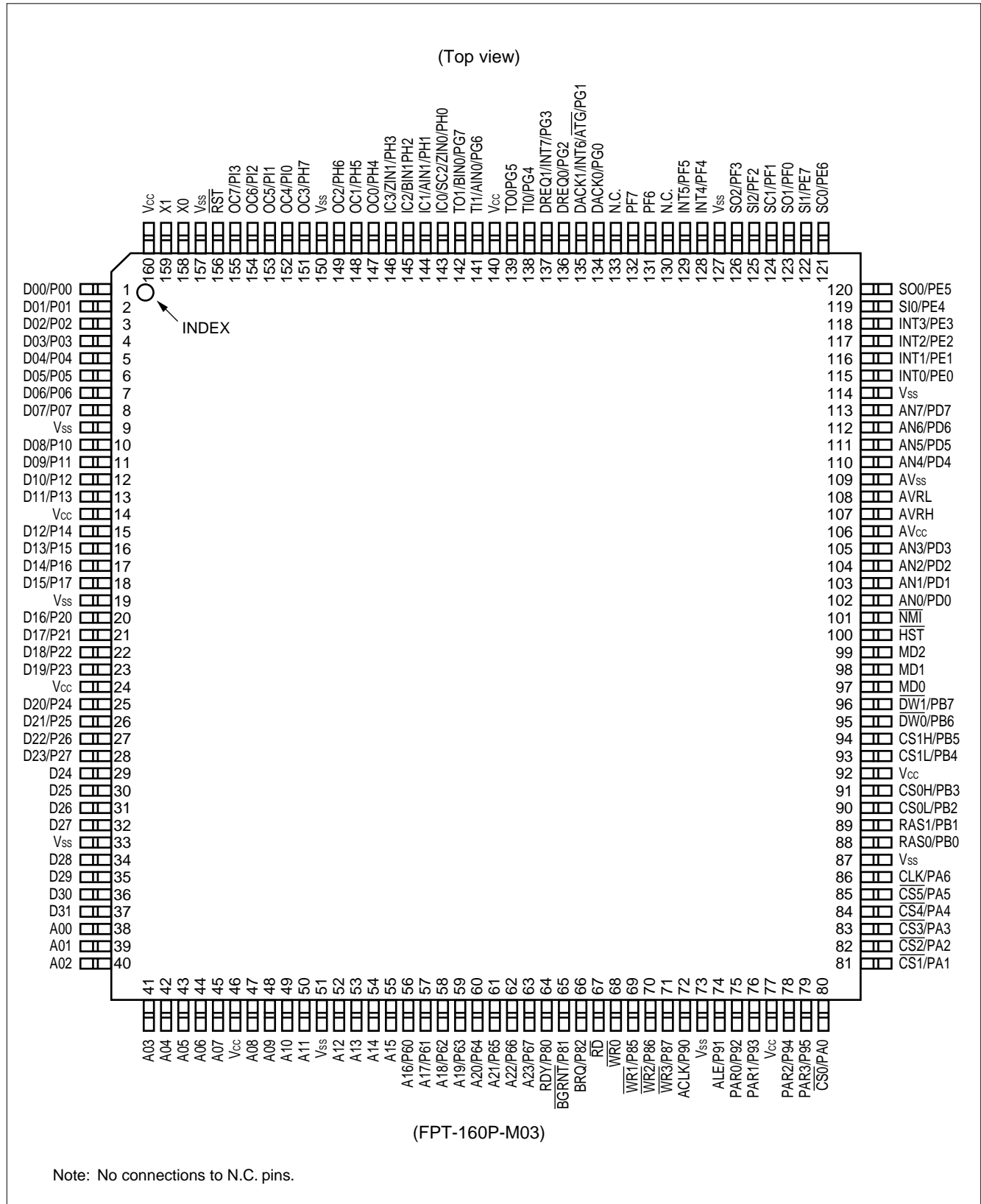
MB91103 Series

■ PRODUCT LINEUP

Product Items	MB91103	MB91V100
Instruction cache	1 KB fixed	Max. 4 KB (4 KB/2 KB/1 KB/512 B selective)
DMAC	5 channels (ch. 0, ch. 1, ch. 4, ch. 5 and ch. 6 only) Address register (32-bit length) × 2 (DMAAR 0, DMAAR 1) Address register (16-bit length) × 6 (DMAAR 2 to DMAAR 7) Transfer count register (16-bit length) × 2 (DMACT 0, DMACT 1) Transfer count register (8-bit length) × 3 (DMACT 4 to DMACT 6) Channels for cycle steal operation: 2 channels (ch. 0, ch. 1) 19 internal transfer causes	8 channels 32-bit length × 4 (DMAAR 0 to DMAAR 3) 16-bit length × 4 (DMAAR 4 to DMAAR 7) 16-bit length × 4 (DMACT 0 to DMACT 3) 8-bit length × 4 (DMACT 4 to DMACT 7) 4 channels (ch. 0 to ch. 3) 23 internal interrupt causes
U-TIMER	2 channels	3 channels
UART	2 channels	3 channels
External interrupts	8 channels (INT0 to INT7)	12 channels (INT0 to INT11)
Timer units		Incorporated
DSP unit		Incorporated
Pin conditions in each state	PG 4 to PG 7 are fixed to 0 when CPU stops	Configured as input when CPU stops

MB91103 Series

PIN ASSIGNMENT



MB91103 Series

■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
QFP*			
158	X0	A	Clock (Oscillator) input
159	X1		Clock (Oscillator) output
97 to 99	MD0 to MD2	G	Mode pins 0 to 2 Input pins for operation mode specification. Directly connect these pins with V_{CC} or V_{SS} for use.
156	\overline{RST}	B	External reset input.
1 to 8	D00 to D07	J	Bit 0 to bit 7 of external data bus.
	P00 to P07		I/O port. This function is available when external data bus width is set to 8-bit or 16-bit.
10 to 13, 15 to 18	D08 to D15	J	Bit 8 to bit 15 of external data bus.
	P10 to P17		I/O port. This function is available when external data bus width is set to 8-bit or 16-bit.
20 to 23, 25 to 28	D16 to D23	J	Bit 16 to bit 23 of external data bus.
	P20 to P27		I/O port. This function is available when external data bus width is set to 8-bit.
29 to 32, 34 to 37	D24 to D31	J	Bit 24 to bit 31 of external data bus.
38 to 45, 47 to 50, 52 to 55	A00 to A15	C	Bit 0 to bit 15 of external address bus.
56 to 63	A16 to A23	C	Bit 16 to bit 23 of external address bus.
	P60 to P67		Can be configured as I/O ports when not used as address bus.
64	RDY	J	External ready input. Outputs "L" level bus cycle is being executed and not completed.
	P80		Can be configured as I/O port.
65	\overline{BGRNT}	C	External bus release acknowledge output. Outputs "L" level when external bus is released.
	P81		Can be configured as I/O port.
66	BRQ	J	External bus release request input. Input "H" level when release of external bus is required.
	P82		Can be configured as I/O port.
67	\overline{RD}	C	Read strobe output pin for external bus.
68	$\overline{WR0}$	C	Write strobe output pin for external bus.

* : FPT-160P-M03

(Continued)

MB91103 Series

Pin No.	Pin name	Circuit type	Function																				
QFP*																							
69 to 71	WR1 to WR3	C	Write strobe output pin for external bus. Relation between control signals and effective byte locations is as follows: <table border="1"> <thead> <tr> <th></th> <th>32-bit bus width</th> <th>16-bit bus width</th> <th>8-bit bus width</th> </tr> </thead> <tbody> <tr> <td>D31 to D24</td> <td>WR0</td> <td>WR0</td> <td>WR0</td> </tr> <tr> <td>D23 to D16</td> <td>WR1</td> <td>WR1</td> <td>(I/O port enabled)</td> </tr> <tr> <td>D15 to D08</td> <td>WR2</td> <td>(I/O port enabled)</td> <td>(I/O port enabled)</td> </tr> <tr> <td>D07 to D00</td> <td>WR3</td> <td>(I/O port enabled)</td> <td>(I/O port enabled)</td> </tr> </tbody> </table>		32-bit bus width	16-bit bus width	8-bit bus width	D31 to D24	WR0	WR0	WR0	D23 to D16	WR1	WR1	(I/O port enabled)	D15 to D08	WR2	(I/O port enabled)	(I/O port enabled)	D07 to D00	WR3	(I/O port enabled)	(I/O port enabled)
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D07 to D00	WR3	(I/O port enabled)	(I/O port enabled)																				
P85 to P87	Can be configured as I/O port.																						
72	ACLK	C	Clock output for a bus cycle.																				
	P90		Can be configured as I/O port.																				
74	ALE	C	Address strobe signal in time-sharing mode.																				
	P91		Can be configured as I/O port.																				
75, 76, 78, 79	PAR0 to PAR3	J	Parity input/output. Relation between control signals and effective byte locations is as follows: <table border="1"> <thead> <tr> <th></th> <th>32-bit bus width</th> <th>16-bit bus width</th> <th>8-bit bus width</th> </tr> </thead> <tbody> <tr> <td>D31 to D24</td> <td>PAR0</td> <td>PAR0</td> <td>PAR0</td> </tr> <tr> <td>D23 to D16</td> <td>PAR1</td> <td>PAR1</td> <td>(I/O port enabled)</td> </tr> <tr> <td>D15 to D08</td> <td>PAR2</td> <td>(I/O port enabled)</td> <td>(I/O port enabled)</td> </tr> <tr> <td>D07 to D00</td> <td>PAR3</td> <td>(I/O port enabled)</td> <td>(I/O port enabled)</td> </tr> </tbody> </table>		32-bit bus width	16-bit bus width	8-bit bus width	D31 to D24	PAR0	PAR0	PAR0	D23 to D16	PAR1	PAR1	(I/O port enabled)	D15 to D08	PAR2	(I/O port enabled)	(I/O port enabled)	D07 to D00	PAR3	(I/O port enabled)	(I/O port enabled)
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D07 to D00	PAR3	(I/O port enabled)	(I/O port enabled)																				
P92 to P95	Can be configured as I/O port.																						
80 to 85	CS0 to CS5	C	Chip select 0 to 5 output ("L" active).																				
	PA0 to PA5		Can be configured as I/O port.																				
86	CLK	C	System clock output. Outputs clock signal of internal operating frequency.																				
	PA6		Can be configured as I/O port.																				
88	RAS0	C	RAS output for DRAM bank 0.																				
	PB0		Can be configured as I/O port.																				
89	RAS1	C	RAS output for DRAM bank 1.																				
	PB1		Can be configured as I/O port.																				
90	CS0L	C	CASL output for DRAM bank 0.																				
	PB2		Can be configured as I/O port.																				
91	CS0H	C	CASH output for DRAM bank 0.																				
	PB3		Can be configured as I/O port.																				
93	CS1L	C	CASL output for DRAM bank 1.																				
	PB4		Can be configured as I/O port.																				

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Pin No.	Pin name	Circuit type	Function
QFP*			
94	CS1H	C	CASH output for DRAM bank 1.
	PB5		Can be configured as I/O port.
95	DW0	C	\overline{WE} output for DRAM bank 0. ("L" active)
	PB6		Can be configured as I/O port.
96	DW1	C	\overline{WE} output for DRAM bank 1. ("L" active)
	PB7		Can be configured as I/O port.
100	HST	H	Directly connects this pin with V_{CC} for use.
101	NMI	H	NMI (non-maskable interrupt pin) input pin. ("L" active)
102 to 105	AN0 to AN3	D	Analog input pins of A/D converter. This function is available when AIC register is set to specify analog input mode.
	PD0 to PD3		General-purpose I/O ports. This function is available when AIC register is set to configure I/O ports.
110 to 113	AN4 to AN7	D	Analog input pins of A/D converter. This function is available when AIC register is set to specify analog input mode.
	PD4 to PD7		General-purpose I/O ports. This function is available when AIC register is set to configure I/O ports.
115 to 118	INT0 to INT3	I	External interrupt request input pins. This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally. INT0 and INT1 can be used as a DMA request when DMAC is so configured.
	PE0 to PE3		General-purpose I/O port.
119	SIO	F	Data input pin for extended serial I/O interface (SIO). This pin is used for input during SIO is in operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PE4		General-purpose I/O port.
120	SO0	C	Data output for extended serial I/O interface (SIO). This function is available when serial data output specification of SIO is enabled.
	PE5		General-purpose I/O port. This function is available when serial data output of extended serial I/O interface (SIO) is disabled.
121	SC0	F	Clock input/output pin for extended serial I/O interface. Clock output is valid when clock output of SIO is enabled.
	PE6		General-purpose I/O port. This function is available when clock output of SIO is enabled.

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Pin No. QFP*	Pin name	Circuit type	Function
122	SI1	F	UART0 data input pin. This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PE7		General-purpose I/O port.
123	SO1	C	UART0 data output pin. This function is available when UART0 data output is enabled.
	PF0		General-purpose I/O port. This function is available when serial data output of UART0 is disabled.
124	SC1	F	UART0 clock I/O pin. This function is available when UART0 clock output is enabled.
	PF1		General-purpose I/O port. This function is available when UART0 clock output is disabled.
125	SI2	F	UART1 data input pin. This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PF2		General-purpose I/O port.
126	SO2	C	UART1 data output pin. This function is available when UART1 data output is enabled.
	PF3		General-purpose I/O port. This function is available when UART1 data output is disabled.
128, 129	INT4, INT5	I	External interrupt request input pins. These pins are used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
	PF4, PF5		General-purpose I/O ports.
131, 132	PF6, PF7	E	I/O ports of open-drain type.
134	DACK0	C	Transfer request acknowledge output pin for DMAC (ch. 0). This function is available when transfer request output for DMAC is enabled.
	PG0		General-purpose I/O port. This function is available when transfer request for DMAC is disabled.

* : FPT-160P-M03

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Pin No.	Pin name	Circuit type	Function
QFP*			
135	DACK1	I	External transfer request acknowledge output pin for DMAC (ch. 1). This function is available when transfer request output for DMAC is enabled.
	INT6		External interrupt request input pins. This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	ATG		External trigger input pin for A/D converter. This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PG1		General-purpose I/O port. This function is available when transfer request acknowledge for DMAC is disabled.
136	DREQ0	F	External transfer request input pin for DMA (ch. 0). This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PG2		General-purpose I/O port.
137	DREQ1	I	External transfer request input pin for DMA (ch. 1). This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	INT7		External interrupt request input pins. This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PG3		General-purpose I/O port.
138	TI0	F	Input pin for reload-timer 0. This pin is used for input when input to reload-timer 0 is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PG4		General-purpose I/O port.
139	TO0	F	Output pin for reload-timer 0. This function is available when output from reload-timer is enabled.
	PG5		General-purpose I/O port. This function is available when output from reload-timer is disabled.

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Pin No.	Pin name	Circuit type	Function
QFP*			
141	TI1	F	Input pin for reload-timer 1. This pin is used for input when input to reload-timer is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	AIN0		AIN input for up/down counter 0. This pin is used for input when input to the counter is enabled in phase-shift count mode or up/down count mode, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PG6		General-purpose I/O port.
142	T01	F	Input pin for reload-timer 1. This pin is used for input when input to reload-timer is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	BIN0		BIN input for up/down counter 0. This pin is used for input when input to the counter is enabled in phase-shift count mode or up/down count mode, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PG7		General-purpose I/O port. This function is available when output from reload-timer is disabled.
143	IC0	F	Input pin for input capture 0 (ICU0). This pin is used for input when ICU is in edge detect operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	SC2		Clock I/O pin for UART1. This function is available when clock output of UART1 is enabled.
	ZIN0		ZIN-input for up/down counter 0. This pin is used for input when ZIN-input to the counter is enabled in by up/down counter 0, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PH0		General purpose I/O port. This function is available when clock output of UART1 is enabled.
144	IC1	F	Input pin for input capture 1 (ICU1). This pin is used for input when ICU is in edge detect operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	AIN1		AIN input for up/down counter 1. This pin is used for input when input to the counter is enabled in phase-shift count mode or up/down count mode, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PH1		General-purpose I/O port.

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Pin No.	Pin name	Circuit type	Function
QFP*			
145	IC2	F	Input pin for input capture 2 (ICU2). This pin is used for input when ICU is in edge detect operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	BIN1		BIN input for up/down counter 1. This pin is used for input when input to the counter is enabled in phase-shift count mode or up/down count mode, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PH2		General-purpose I/O port.
146	IC3	F	Input pin for input capture 3 (ICU3). This pin is used for input when ICU is in edge detect operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	ZIN1		ZIN-input for up/down counter 1. This pin is used for input when ZIN-input to the counter is enabled by up/down counter 1, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
	PH3		General-purpose I/O port.
147	OC0	K	Output pin for output compare 0 (OCU0). This function is available when output of corresponding OCU is enabled.
	PH4		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
148	OC1	K	Output pin for output compare 1 (OCU1). This function is available when output of corresponding OCU is enabled.
	PH5		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
149	OC2	K	Output pin for output compare 2 (OCU2). This function is available when output of corresponding OCU is enabled.
	PH6		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
151	OC3	K	Output pin for output compare 3 (OCU3). This function is available when output of corresponding OCU is enabled.
	PH7		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.

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Pin No.	Pin name	Circuit type	Function
QFP*			
152	OC4	K	Output pin for output compare 4 (OCU4). This function is available when output of corresponding OCU is enabled.
	PI0		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
153	OC5	K	Output pin for output compare 5 (OCU5). This function is available when output of corresponding OCU is enabled.
	PI1		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
154	OC6	K	Output pin for output compare 6 (OCU6). This function is available when output of corresponding OCU is enabled.
	PI2		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
155	OC7	F	Output pin for output compare 7 (OCU7). This function is available when output of corresponding OCU is enabled.
	PI3		General-purpose I/O port. This function is available when output of corresponding OCU is disabled.
130, 133	N.C.	—	No connections allowed to this pin.
14, 24 46, 77 92, 140 160	V _{cc}	—	Power supply pin (V _{cc}) for digital circuit
9, 19 33, 51 73, 87 114, 127 150, 157	V _{ss}	—	Earth level (V _{ss}) for digital circuit.
106	AV _{cc}	—	Power supply pin (V _{cc}) for A/D converter.
107	AVRH	—	Reference voltage input (High) for A/D converter. Make sure to turn on and off this pin with potential of AVRH or more applied to V _{cc} .
108	AVRL	—	Reference voltage input pin (Low) for A/D converter.
109	AV _{ss}	—	Power supply pin (V _{ss}) for A/D converter.

* : FPT-160P-M03

Note: In most of the above pins, I/O port and resource I/O are multiplexed e.g. P82 and BRQ. In case of conflict between output of I/O port and resource I/O, priority is always given to the output of resource I/O.

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■ DRAM CONTROL PIN

Pin name	Data bus 32-bit mode		Data bus 16-bit mode		Data bus 8-bit mode
	2CAS/1WE mode	1CAS/2WE mode	2CAS/1WE mode	1CAS/2WE mode	—
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Area 4 RAS	Area 4 RAS
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	Area 5 RAS	Area 5 RAS
CS0L	CAS0 *1	CAS	Area 4 CASL *2	Area 4 CAS	Area 4 CAS
CS0H	CAS1 *1	CAS	Area 4 CASH *2	Area 4 \overline{WEL} *2	Area 4 CAS
CS1L	CAS2 *1	$\overline{WE0}$ *1	Area 5 CASL *2	Area 5 CAS	Area 5 CAS
CS1H	CAS3 *1	$\overline{WE1}$ *1	Area 5 CASH *2	Area 5 \overline{WEL} *2	Area 5 CAS
$\overline{DW0}$	\overline{WE}	$\overline{WE2}$ *1	Area 4 \overline{WE}	Area 4 \overline{WEH} *2	Area 4 \overline{WE}
$\overline{DW1}$	\overline{WE}	$\overline{WE3}$ *1	Area 5 \overline{WE}	Area 5 \overline{WEH} *2	Area 5 \overline{WE}

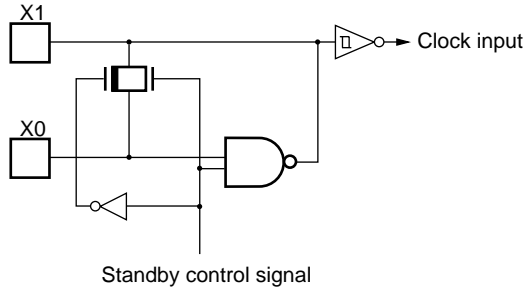
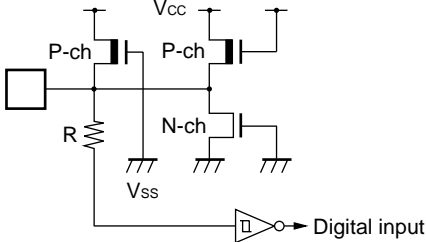
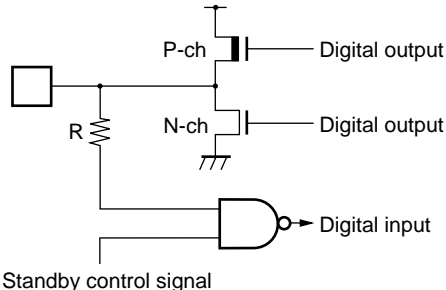
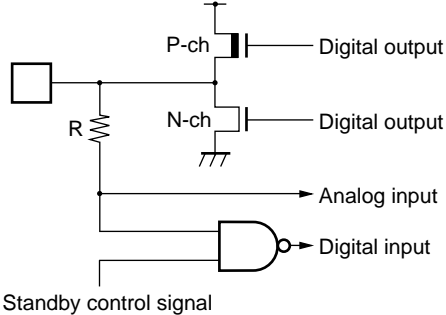
*1: 0, 1, 2 and 3 respectively corresponds to the lowest 2 bits of address as follows:

0: "00", 1: "01", 2: "10", 3: "11"

*2: L and H respectively corresponds to the LSB of address as follows:

L: "0", H: "1"

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> Oscillation feedback resistance 1 MΩ approx. With Standby control
B	 <p style="text-align: right;">Digital input</p>	<ul style="list-style-type: none"> CMOS level hysteresis input Without standby control With pull-up resistance
C	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> CMOS level I/O With standby control
D	 <p style="text-align: center;">Standby control signal</p>	<ul style="list-style-type: none"> CMOS level I/O With standby control Analog input

(Continued)

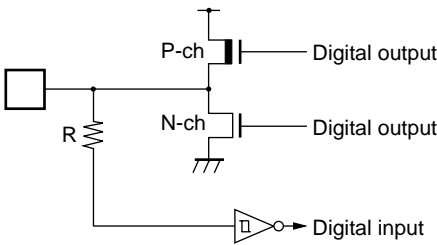
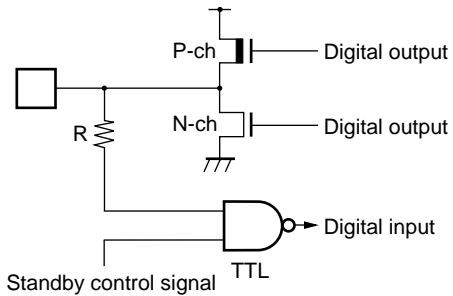
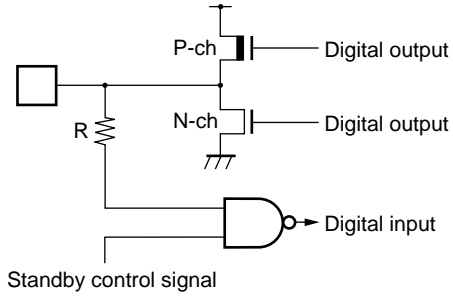
MB91103 Series

Type	Circuit	Remarks
E		<ul style="list-style-type: none"> • N-ch open-drain output • CMOS level output • With standby control
F		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby control
G		<ul style="list-style-type: none"> • CMOS level I/O • Without standby control
H		<ul style="list-style-type: none"> • CMOS level hysteresis input • Without standby control

(Continued)

MB91103 Series

(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input Without standby control
J		<ul style="list-style-type: none"> • CMOS level output • TTL level input With standby control
K		<ul style="list-style-type: none"> • CMOS level input/output With standby control • Large current drive

MB91103 Series

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

For the same reason, make sure to prevent the analog power supply voltage (AV_{CC} , AVR) and analog input from exceeding the digital power supply voltage when turning on/off the device.

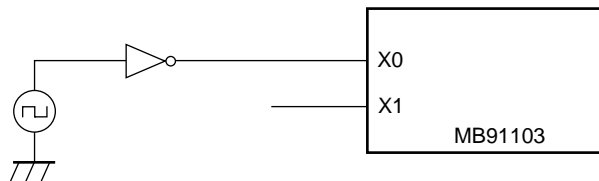
2. Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

3. Remarks for External Clock Operation

When external clock is selected, stabilization time is necessary at the time of power reset (optional) or waking up from stop mode.

• Using an External Clock



4. Power Supply Pins

When there are several V_{CC} and V_{SS} pins, each of them is geometrically connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect each pin directly to V_{CC} or V_{SS} outside of the device.

It is preferred to connect V_{CC} and V_{SS} of this device to power supply with minimal impedance possible.

It is also recommended to connect a bypass capacitor of about $0.1 \mu\text{F}$ between V_{CC} and V_{SS} at a position as close as possible to this device.

5. Crystal Oscillator Circuit

Noises around X0 and X1 pins may cause malfunctions of this device. In designing the PC board, lay out X0, X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible. Prevent their wiring from being crossed by other wires.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

6. Turning-on Sequence of A/D Converter Power Supply and Analog Input

Make sure to turn on the digital power supply (V_{CC}) before turning on the A/D converter (AV_{CC} , AV_{RH} , AV_{RL}) and applying voltage to analog input (AN0 to AN7).

Make sure to turn off digital power supply after power supply to A/D converters and analog inputs have been switched off. (There are no such limitations in turning on power supplies. Analog and digital power supplies may be turned on simultaneously.) Make sure that AV_{RH} never exceeds AV_{CC} when turning on/off power supplies.

7. Treatment of N.C. Pins

Make sure to leave N.C. (internal connection) pins open.

8. Fluctuation of Power Supply Voltage

Warranty range for normal operation against fluctuation of power supply voltage is as given in rating. However, sudden fluctuation of power supply voltage within the warranty range may cause malfunctions. It is recommended to make every effort to stabilize the power supply voltage.

9. Mode Setting Pins

Connect mode setting pins (MD0 to MD2) directly to V_{CC} or V_{SS} .

Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

10. External Reset Input

Keep the \overline{RST} pin level at "L" for at least 5 machine cycles to ensure proper reset operation.

11. I/O Access Limitations When Using Gear Function

In MB91103 series, there are some limitations concerning about accesses to the I/O area.

Limited I/O area: $0X10_H$ to $0XFF_H$
 $0X400_H$ to $0X5FF_H$

Clock gear combinations:

Peripheral system CPU system	1/1	1/2	1/4	1/8
1/1	○	△	△	△
1/2	△	○	△	△
1/4	○	△	○	△
1/8	○	○	△	○

○ : Without limitation

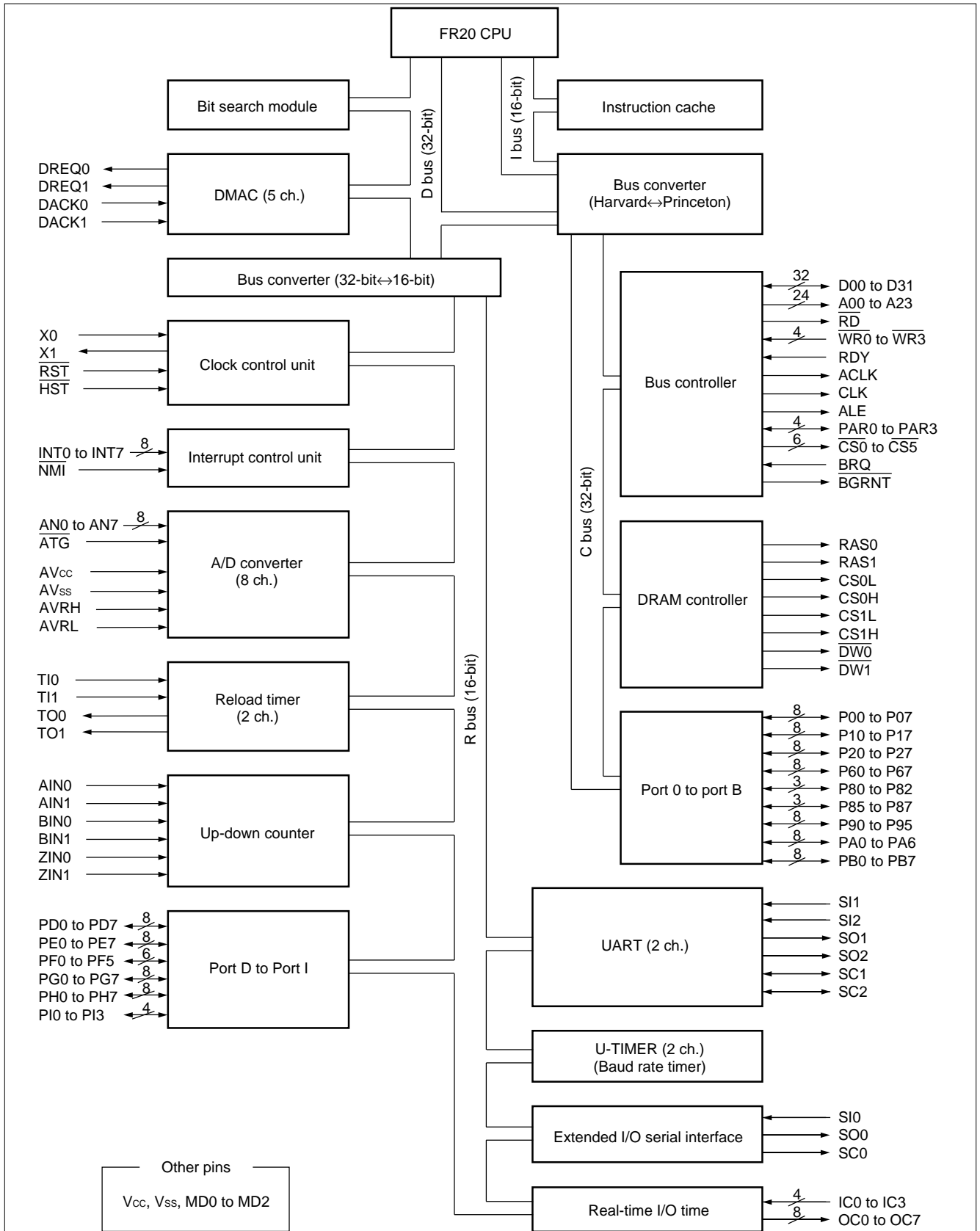
△ : Limited

In the limited clock gear combination shown in the above table, there are limitations concerning about accesses to the applicable I/O area as below.

- (1) When accessing to the I/O area, use only 16-bit length instruction or 8-bit length instruction.
- (2) When putting the read-out instruction from the applicable I/O area right after the write-in instruction to the same I/O area, put the dummy read-out instruction from the same area.

MB91103 Series

■ BLOCK DIAGRAM



MB91103 Series

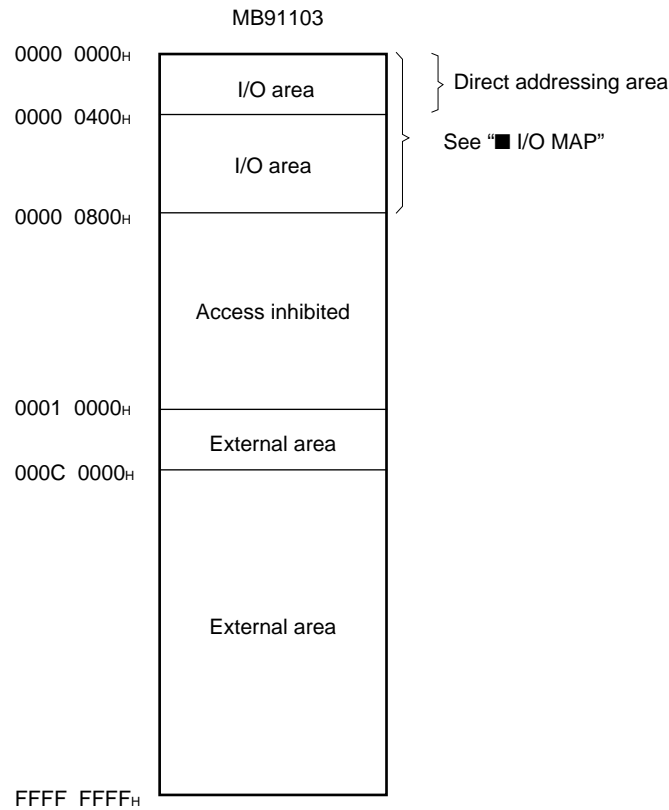
■ CPU CORE

1. Memory Space

The FR20 series has a logical address space of 4 G bytes (2^{32} bytes) and the CPU linearly accesses the memory space.

The MB91103 has no internal memories (RAM, ROM).

• Memory space



• Direct addressing area

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consists of the following areas dependent on accessible data sizes.

Byte data access: 0 to 0FF_H

Half word data access: 0 to 1FF_H

Word data access: 0 to 3FF_H

MB91103 Series

2. Registers

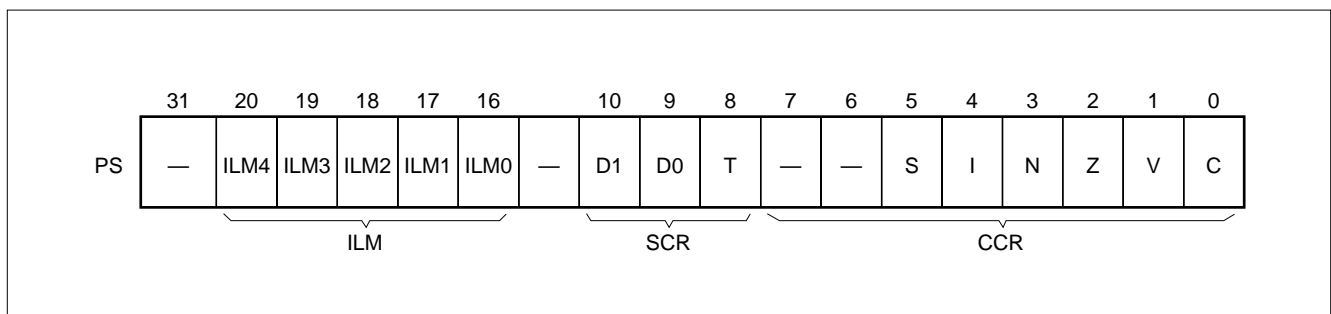
The FR20 series has two types of registers -- dedicated registers embedded on the CPU and general-purpose registers on memory.

- Dedicated registers

- Program counter (PC) : 32-bit length, indicates the location of the instruction to be executed
- Program status (PS) : 32-bit length, register for storing register pointer or condition codes
- Table base register (TBR) : Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
- Return pointer (RP) : Holds address to resume operation after returning from a subroutine.
- System stack pointer (SSP) : Indicates system stack space.
- User's stack pointer (USP) : Indicates user's stack space.
- Multiplication/Division result register (MDH/MDL): 32-bit length, register for multiplication/division.

← 32 bits →		Initial value
PC	Program counter	XXXX XXXX _H not fixed
PS	Program status	
TBR	Table base register	000F FC00 _H
RP	Return pointer	XXXX XXXX _H not fixed
SSP	System stack pointer	0000 0000 _H
USP	User's stack pointer	XXXX XXXX _H not fixed
MDH	Multiplication/division result register	XXXX XXXX _H not fixed
MDL		XXXX XXXX _H not fixed

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a level mask register (ILM).



MB91103 Series

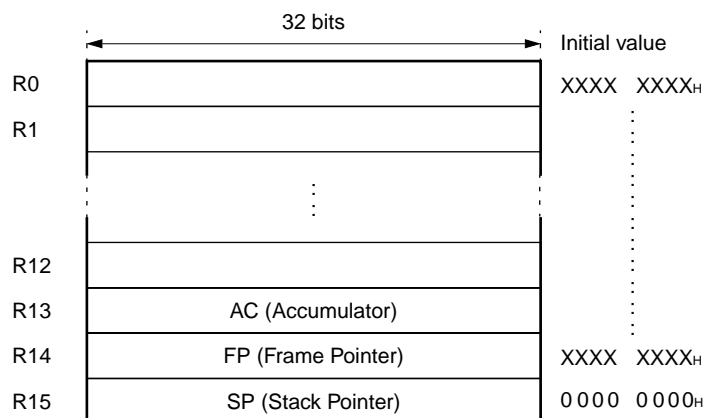
- Condition code register (CCR)
 - S flag : Specifies a stack pointer used as R15.
 - I flag : Controls user interrupt request enable/disable.
 - N flag : Indicates sign bit when division result is assumed to be in the 2's complement format.
 - Z flag : Indicates whether or not the result of division was "0".
 - V flag : Assume the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.
 - C flag : Indicates if a carry or borrow from the MSB has occurred.
- System condition code register (SCR)
 - T flag : Specifies whether or not to enable step trace trap.
- Interrupt level mask register (ILM)
 - ILM4 to ILM0 : Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	Priority
0	0	0	0	0	0	High
⋮					⋮	↑ ↓ Low
0	1	0	0	0	15	
⋮					⋮	
1	1	1	1	1	31	

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address). User can specify the functions of the registers.

• Register bank structure



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

R13: Virtual accumulator (AC)

R14: Frame pointer (FP)

R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 00000000_H (SSP value).

MB91103 Series

■ SETTING MODE

1. Pin

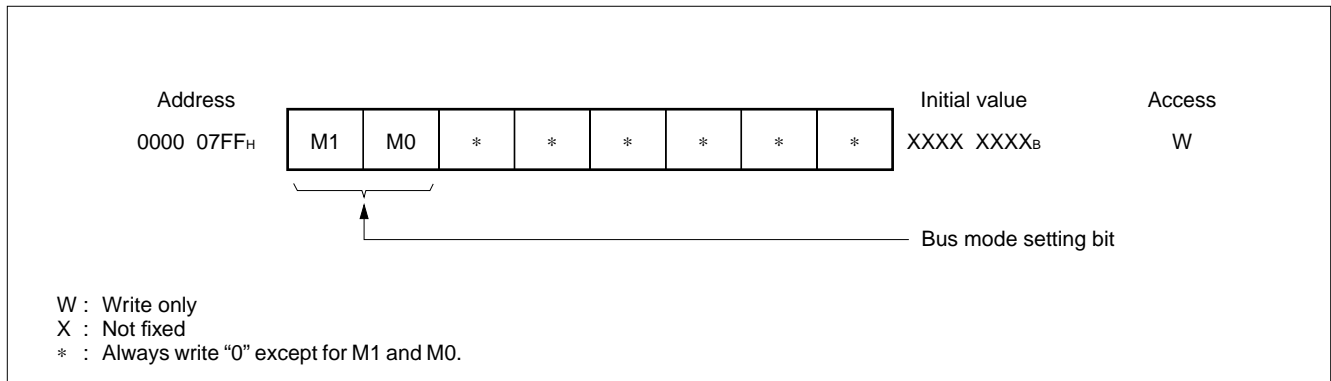
• Mode setting pins and modes

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM External bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	External vector mode 2	External	32 bits	
0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Inhibited

* : MB91103 does not support single-chip mode.

2. Registers

• Mode setting registers and modes



• Bus mode setting bits and functions

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM external bus mode	
1	0	External ROM External bus mode	
1	1	—	Inhibited

Note: For a device without internal ROM, set "10_B" only.
MB91103 allows "10_B" setting only.

MB91103 Series

■ I/O MAP

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
0000 _H		Vacant		
0001 _H	PDR2	Port 2 data register	R/W	XXXXXXXX _B
0002 _H	PDR1	Port 1 data register	R/W	XXXXXXXX _B
0003 _H	PDR0	Port 0 data register	R/W	XXXXXXXX _B
0004 _H		Vacant		
0005 _H	PDR6	Port 6 data register	R/W	XXXXXXXX _B
0006 _H		Vacant		
0007 _H				
0008 _H	PDRB	Port B data register	R/W	XXXXXXXX _B
0009 _H	PDRA	Port A data register	R/W	-XXXXXXXX _B
000A _H	PDR9	Port 9 data register	R/W	--XXXXXXXX _B
000B _H	PDR8	Port 8 data register	R/W	XXX--XXX _B
000C _H to 0010 _H		Vacant		
0011 _H	PDRD	Port D data register	R/W	XXXXXXXX _B
0012 _H	PDRE	Port E data register	R/W	XXXXXXXX _B
0013 _H	PDRF	Port F data register	R/W	XXXXXXXX _B
0014 _H	PDRG	Port G data register	R/W	XXXXXXXX _B
0015 _H	PDRH	Port H data register	R/W	XXXXXXXX _B
0016 _H	PDRI	Port I data register	R/W	----XXXX _B
0017 _H		Vacant		
0018 _H				
0019 _H	SDR	Serial data register	R/W	XXXXXXXX _B
001A _H	SMCS	Serial mode control status register	R/W	0000010 _B
001B _H				----0000 _B
001C _H	SSR0	Serial status register 0	R/W	00001-00 _B
001D _H	SIDR0/SODR0	Serial input register 0/Serial output register 0	R/W	XXXXXXXX _B
001E _H	SCR0	Serial control register 0	R/W	00000100 _B
001F _H	SMR0	Serial mode register 0	R/W	00--0-00 _B
0020 _H	SSR1	Serial status register 1	R/W	00001-00 _B
0021 _H	SIDR1/SODR1	Serial input register 1/Serial output register 1	R/W	XXXXXXXX _B
0022 _H	SCR1	Serial control register 1	R/W	00000100 _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
0023 _H	SMR1	Serial mode register 1	R/W	00--0-00 _B
0024 _H to 0027 _H	Vacant			
0028 _H	TMRLR0	16-bit reload register ch. 0	W	XXXXXXXX _B
0029 _H				XXXXXXXX _B
002A _H	TMR0	16-bit timer register ch. 0	R	XXXXXXXX _B
002B _H				XXXXXXXX _B
002C _H 002D _H	Vacant			
002E _H	TMCSR0	16-bit reload timer control status register ch. 0	R/W	----0000 _B
002F _H				00000000 _B
0030 _H	TMRLR1	16-bit reload register ch. 1	W	XXXXXXXX _B
0031 _H				XXXXXXXX _B
0032 _H	TMR1	16-bit timer register ch. 1	R	XXXXXXXX _B
0033 _H				XXXXXXXX _B
0034 _H 0035 _H	Vacant			
0036 _H	TMCSR1	16-bit reload timer control status register ch. 1	R/W	----0000 _B
0037 _H				00000000 _B
0038 _H	ADCR	A/D converter data register	R	000000XX _B
0039 _H				XXXXXXXX _B
003A _H	ADCS	A/D converter control status register	R/W	00000000 _B
003B _H				00000000 _B
003C _H to 0044 _H	Vacant			
0045 _H	ICS0	Input capture control status register ch. 0	R/W	00000000 _B
0046 _H 0047 _H	Vacant			
0048 _H	IPCP0	Input capture data register 0	R	XXXXXXXX _B
0049 _H				XXXXXXXX _B
004A _H	IPCP1	Input capture data register 1	R	XXXXXXXX _B
004B _H				XXXXXXXX _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
004C _H		Vacant		
004D _H	ICS1	Input capture control status register ch. 1	R/W	0 0 0 0 0 0 0 0 _B
004F _H		Vacant		
004E _H				
0050 _H	IPCP2	Input capture data register 2	R	XXXXXXXX _B
0051 _H				XXXXXXXX _B
0052 _H	IPCP3	Input capture data register 3	R	XXXXXXXX _B
0053 _H				XXXXXXXX _B
0054 _H	OCS0	Output compare control status register ch. 0	R/W	---00000 _B
0055 _H				0000--00 _B
0056 _H		Vacant		
0057 _H				
0058 _H	OPCP0	Output compare register ch. 0	R/W	XXXXXXXX _B
0059 _H				XXXXXXXX _B
005A _H	OPCP1	Output compare register ch. 1	R/W	XXXXXXXX _B
005B _H				XXXXXXXX _B
005C _H	OCS1	Output compare control status register ch. 1	R/W	---00000 _B
005D _H				0000--00 _B
005E _H		Vacant		
005F _H				
0060 _H	OPCP2	Output compare register ch. 2	R/W	XXXXXXXX _B
0061 _H				XXXXXXXX _B
0062 _H	OPCP3	Output compare register ch. 3	R/W	XXXXXXXX _B
0063 _H				XXXXXXXX _B
0064 _H	OCS2	Output compare control status register ch. 2	R/W	---00000 _B
0065 _H				0000--00 _B
0066 _H		Vacant		
0067 _H				
0068 _H	OPCP4	Output compare register ch. 4	R/W	XXXXXXXX _B
0069 _H				XXXXXXXX _B
006A _H	OPCP5	Output compare register ch. 5	R/W	XXXXXXXX _B
006B _H				XXXXXXXX _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
006C _H	OCS3	Output compare control status register ch. 3	R/W	---00000 _B
006D _H				0000--00 _B
006E _H	Vacant			
006F _H				
0070 _H	OPCP6	Output compare register ch. 6	R/W	XXXXXXXX _B
0071 _H				XXXXXXXX _B
0072 _H	OPCP7	Output compare register ch. 7	R/W	XXXXXXXX _B
0073 _H				XXXXXXXX _B
0074 _H	TCDT	16-bit free-run timer count data register	R/W	00000000 _B
0075 _H				00000000 _B
0076 _H	Vacant			
0077 _H	TCCS	16-bit free-run timer count control status register	R/W	00000000 _B
0078 _H	UTIM0/UTIMR0	U-TIMER register ch. 0/Reload register ch. 0	R/W	00000000 _B
0079 _H				00000000 _B
007A _H	Vacant			
007B _H	UTIMC0	U-TIMER control register ch. 0	R/W	0--00001 _B
007C _H	UTIM1/UTIMR1	U-TIMER register ch. 1/Reload register ch. 1	R/W	00000000 _B
007D _H				00000000 _B
007E _H	Vacant			
007F _H	UTIMC1	U-TIMER control register ch. 1	R/W	0--00001 _B
0080 _H to 0083 _H	Vacant			
0084 _H	UDCR0	16-bit up-down count register ch. 0	R	00000000 _B
0085 _H				00000000 _B
0086 _H	RCR0	16-bit up/down counter reload/compare register ch. 0	W	00000000 _B
0087 _H				00000000 _B
0088 _H	CCR0	16-bit up/down counter control register ch. 0	R/W	-0000000 _B
0089 _H				-0001000 _B
008A _H	Vacant			
008B _H	CSR0	16-bit up/down counter status register ch. 0	R/W	00000000 _B
008C _H	UDCR1	16-bit up/down count register ch. 1	R	00000000 _B
008D _H				00000000 _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
008E _H	RCR1	16-bit up/down counter reload/compare register ch. 1	W	0 0 0 0 0 0 0 0 _B
008F _H				0 0 0 0 0 0 0 0 _B
0090 _H	CCR1	16-bit up/down counter control register ch. 1	R/W	- 0 0 0 0 0 0 0 _B
0091 _H				- 0 0 0 1 0 0 0 _B
0092 _H	Vacant			
0093 _H	CSR1	16-bit up/down counter status register ch. 1	R/W	0 0 0 0 0 0 0 0 _B
0094 _H	EIRR	External interrupt cause register	R/W	0 0 0 0 0 0 0 0 _B
0095 _H	ENIR	Interrupt enable register	R/W	0 0 0 0 0 0 0 0 _B
0096 _H	Vacant			
0097 _H				
0098 _H	ELVR	External interrupt request level setting register	R/W	0 0 0 0 0 0 0 0 _B
0099 _H				0 0 0 0 0 0 0 0 _B
009A _H to 00D0 _H	Vacant			
00D1 _H	DDRD	Port D data direction register	W	0 0 0 0 0 0 0 0 _B
00D2 _H	DDRE	Port E data direction register	W	0 0 0 0 0 0 0 0 _B
00D3 _H	DDRF	Port F data direction register	W	0 0 0 0 0 0 0 0 _B
00D4 _H	DDRG	Port G data direction register	W	0 0 0 0 0 0 0 0 _B
00D5 _H	DDRH	Port H data direction register	W	0 0 0 0 0 0 0 0 _B
00D6 _H	DDRI	Port I data direction register	W	- - - - 0 0 0 0 _B
00D7 _H	AIC	Port D analog input control register	W	0 0 0 0 0 0 0 0 _B
00D8 _H to 01FF _H	Vacant			
0200 _H	DMACS0	DMAC-ch. 0 control/status register	R/W	0 - 0 0 0 0 0 0 _B
0201 _H				0 0 0 - - - X 0 _B
0202 _H				X X X X X X X X _B
0203 _H				X X X X X X - X _B
0204 _H	DMACC0	DMAC-ch. 0 addressing/count setting register	R/W	X X X X X X X X _B
0205 _H				- X X X X X X X _B
0206 _H				X X X X X X X X _B
0207 _H				X X X X X X X X _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
0208 _H	DMACS1	DMAC-ch. 1 control/status register	R/W	0-000000 _B
0209 _H				000---X0 _B
020A _H				XXXXXXXX _B
020B _H				XXXXXXXX-X _B
020C _H	DMACC1	DMAC-ch. 1 addressing/count setting register	R/W	XXXXXXXX _B
020D _H				-XXXXXXXX _B
020E _H				XXXXXXXX _B
020F _H				XXXXXXXX _B
0210 _H to 021F _H	Vacant			
0220 _H	DMACS4	DMAC-ch. 4 control/status register	R/W	0-000000 _B
0221 _H				000----- _B
0222 _H				--XXXXXXXX _B
0223 _H				----XX-X _B
0224 _H	DMACC4	DMAC-ch. 4 addressing/count setting register	R/W	0000XXXX _B
0225 _H				-XXXXXXXX _B
0226 _H				XXXXXXXX _B
0227 _H				XXXXXXXX _B
0228 _H	DMACS5	DMAC-ch. 5 control/status register	R/W	0-000000 _B
0229 _H				000----- _B
022A _H				--XXXXXXXX _B
022B _H				----XX-X _B
022C _H	DMACC5	DMAC-ch. 5 addressing/count setting register	R/W	0000XXXX _B
022D _H				-XXXXXXXX _B
022E _H				XXXXXXXX _B
022F _H				XXXXXXXX _B
0230 _H	DMACS6	DMAC-ch. 6 control/status register	R/W	0-000000 _B
0231 _H				000----- _B
0232 _H				--XXXXXXXX _B
0233 _H				----XX-X _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
0234 _H	DMAACC6	DMAC-ch. 6 addressing/count setting register	R/W	0 0 0 0 X X X X _B
0235 _H				- X X X X X X X _B
0236 _H				X X X X X X X X _B
0237 _H				X X X X X X X X _B
0238 _H to 023F _H	Vacant			
0240 _H	DMAAR0	DMAC address register 0	R/W	X X X X X X X X _B
0241 _H				X X X X X X X X _B
0242 _H				X X X X X X X X _B
0243 _H				X X X X X X X X _B
0244 _H	DMAAR1	DMAC address register 1	R/W	X X X X X X X X _B
0245 _H				X X X X X X X X _B
0246 _H				X X X X X X X X _B
0247 _H				X X X X X X X X _B
0248 _H	DMAAR2	DMAC address register 2	R/W	0 0 0 0 0 0 0 0 _B
0249 _H				0 0 0 0 0 X X X _B
024A _H				X X X X X X X X _B
024B _H				X X X X X X X X _B
024C _H	DMAAR3	DMAC address register 3	R/W	0 0 0 0 0 0 0 0 _B
024D _H				0 0 0 0 0 X X X _B
024E _H				X X X X X X X X _B
024F _H				X X X X X X X X _B
0250 _H	DMAAR4	DMAC address register 4	R/W	0 0 0 0 0 0 0 0 _B
0251 _H				0 0 0 0 0 X X X _B
0252 _H				X X X X X X X X _B
0253 _H				X X X X X X X X _B
0254 _H	DMAAR5	DMAC address register 5	R/W	0 0 0 0 0 0 0 0 _B
0255 _H				0 0 0 0 0 X X X _B
0256 _H				X X X X X X X X _B
0257 _H				X X X X X X X X _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
0258 _H	DMAAR6	DMAC address register 6	R/W	0 0 0 0 0 0 0 0 _B
0259 _H				0 0 0 0 0 X X X _B
025A _H				X X X X X X X X _B
025B _H				X X X X X X X X _B
025C _H	DMAAR7	DMAC address register 7	R/W	0 0 0 0 0 0 0 0 _B
025D _H				0 0 0 0 0 X X X _B
025E _H				X X X X X X X X _B
025F _H				X X X X X X X X _B
0260 _H	DMACT0	DMAC transfer count register 0	R/W	X X X X X X X X _B
0261 _H				X X X X X X X X _B
0262 _H	DMACT1	DMAC transfer count register 1	R/W	X X X X X X X X _B
0263 _H				X X X X X X X X _B
0264 _H to 0267 _H	Vacant			
0268 _H	DMACT4	DMAC transfer count register 4	R/W	0 0 0 0 0 0 0 0 _B
0269 _H				X X X X X X X X _B
026A _H	DMACT5	DMAC transfer count register 5	R/W	0 0 0 0 0 0 0 0 _B
026B _H				X X X X X X X X _B
026C _H	DMACT6	DMAC transfer count register 6	R/W	0 0 0 0 0 0 0 0 _B
026D _H				X X X X X X X X _B
026E _H to 0273 _H	Vacant			
0274 _H	DMACT6	DMAC total control register	R/W	----- _B
0275 _H				----- _B
0276 _H				00----- _B
0277 _H				----0000 _B
0278 _H to 03E3 _H	Vacant			
03E4 _H	ICHCR	Instruction cache control register	R/W	----- _B
03E5 _H				----- _B
03E6 _H				----- _B
03E7 _H				--000000 _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
03E8 _H to 03EF _H		Vacant		
03F0 _H	BSD0	Bit search module 0-detection data register	W	XXXXXXXX _B
03F1 _H				XXXXXXXX _B
03F2 _H				XXXXXXXX _B
03F3 _H				XXXXXXXX _B
03F4 _H	BSD1	Bit search module 1-detection data register	R/W	XXXXXXXX _B
03F5 _H				XXXXXXXX _B
03F6 _H				XXXXXXXX _B
03F7 _H				XXXXXXXX _B
03F8 _H	BSDC	Bit search module transition-detection data register	W	XXXXXXXX _B
03F9 _H				XXXXXXXX _B
03FA _H				XXXXXXXX _B
03FB _H				XXXXXXXX _B
03FC _H	BSRR	Bit search module detection result register	R	XXXXXXXX _B
03FD _H				XXXXXXXX _B
03FE _H				XXXXXXXX _B
03FF _H				XXXXXXXX _B
0400 _H	ICR00	Interrupt control register 0	R/W	---1111 _B
0401 _H	ICR01	Interrupt control register 1	R/W	---1111 _B
0402 _H	ICR02	Interrupt control register 2	R/W	---1111 _B
0403 _H	ICR03	Interrupt control register 3	R/W	---1111 _B
0404 _H	ICR04	Interrupt control register 4	R/W	---1111 _B
0405 _H	ICR05	Interrupt control register 5	R/W	---1111 _B
0406 _H	ICR06	Interrupt control register 6	R/W	---1111 _B
0407 _H	ICR07	Interrupt control register 7	R/W	---1111 _B
0408 _H	ICR08	Interrupt control register 8	R/W	---1111 _B
0409 _H	ICR09	Interrupt control register 9	R/W	---1111 _B
040A _H	ICR10	Interrupt control register 10	R/W	---1111 _B
040B _H	ICR11	Interrupt control register 11	R/W	---1111 _B
040C _H	ICR12	Interrupt control register 12	R/W	---1111 _B
040D _H	ICR13	Interrupt control register 13	R/W	---1111 _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
040E _H	ICR14	Interrupt control register 14	R/W	---11111 _B
040F _H	ICR15	Interrupt control register 15	R/W	---11111 _B
0410 _H	ICR16	Interrupt control register 16	R/W	---11111 _B
0411 _H	ICR17	Interrupt control register 17	R/W	---11111 _B
0412 _H	ICR18	Interrupt control register 18	R/W	---11111 _B
0413 _H	ICR19	Interrupt control register 19	R/W	---11111 _B
0414 _H	ICR20	Interrupt control register 20	R/W	---11111 _B
0415 _H	ICR21	Interrupt control register 21	R/W	---11111 _B
0416 _H	ICR22	Interrupt control register 22	R/W	---11111 _B
0417 _H	ICR23	Interrupt control register 23	R/W	---11111 _B
0418 _H	ICR24	Interrupt control register 24	R/W	---11111 _B
0419 _H	ICR25	Interrupt control register 25	R/W	---11111 _B
041A _H	ICR26	Interrupt control register 26	R/W	---11111 _B
041B _H	ICR27	Interrupt control register 27	R/W	---11111 _B
041C _H	ICR28	Interrupt control register 28	R/W	---11111 _B
041D _H	ICR29	Interrupt control register 29	R/W	---11111 _B
041E _H	ICR30	Interrupt control register 30	R/W	---11111 _B
041F _H	ICR31	Interrupt control register 31	R/W	---11111 _B
0420 _H	ICR32	Interrupt control register 32	R/W	---11111 _B
0421 _H	ICR33	Interrupt control register 33	R/W	---11111 _B
0422 _H	ICR34	Interrupt control register 34	R/W	---11111 _B
0423 _H	ICR35	Interrupt control register 35	R/W	---11111 _B
0424 _H	ICR36	Interrupt control register 36	R/W	---11111 _B
0425 _H	ICR37	Interrupt control register 37	R/W	---11111 _B
0426 _H	ICR38	Interrupt control register 38	R/W	---11111 _B
0427 _H	ICR39	Interrupt control register 39	R/W	---11111 _B
0428 _H	ICR40	Interrupt control register 40	R/W	---11111 _B
0429 _H	ICR41	Interrupt control register 41	R/W	---11111 _B
042A _H	ICR42	Interrupt control register 42	R/W	---11111 _B
042B _H	ICR43	Interrupt control register 43	R/W	---11111 _B
042C _H	ICR44	Interrupt control register 44	R/W	---11111 _B
042D _H	ICR45	Interrupt control register 45	R/W	---11111 _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
042E _H	ICR46	Interrupt control register 46	R/W	---11111 _B
042F _H	ICR47	Interrupt control register 47	R/W	---11111 _B
0430 _H	DICR	Delayed interrupt control register	R/W	-----0 _B
0431 _H	HRCL	Hold request cancel request level setting register	R/W	---11111 _B
0432 _H to 047F _H	Vacant			
0480 _H	RSRR/WTCR	Reset cause register/Watch-dog peripheral control register	R/W	1-XXX-00 _B
0481 _H	STCR	Standby control register	R/W	000111-- _B
0482 _H	PDRR	DMA request squelch register	R/W	----0000 _B
0483 _H	CTBR	Time-base timer clear register	W	XXXXXXXX _B
0484 _H	GCR	Gear control register	R/W	11--11-1 _B
0485 _H	WPR	Watch-dog reset occurrence postpone register	W	XXXXXXXX _B
0486 _H to 0600 _H	Vacant			
0601 _H	DDR2	Port 2 data direction register	W	00000000 _B
0602 _H	DDR1	Port 1 data direction register	W	00000000 _B
0603 _H	DDR0	Port 0 data direction register	W	00000000 _B
0604 _H	Vacant			
0605 _H	DDR6	Port 6 data direction register	W	00000000 _B
0606 _H 0607 _H	Vacant			
0608 _H	DDRB	Port B data direction register	W	00000000 _B
0609 _H	DDRA	Port A data direction register	W	-0000000 _B
060A _H	DDR9	Port 9 data direction register	W	--000000 _B
060B _H	DDR8	Port 8 data direction register	W	000--000 _B
060C _H 060D _H	ASR1	Area select register 1	W	00000000 _B
				00000001 _B
060E _H 060F _H	AMR1	Area mask register 1	W	00000000 _B
				00000000 _B
0610 _H 0611 _H	ASR2	Area select register 2	W	00000000 _B
				00000010 _B

(Continued)

MB91103 Series

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
0612 _H	AMR2	Area mask register 2	W	0 0 0 0 0 0 0 0 _B
0613 _H				0 0 0 0 0 0 0 0 _B
0614 _H	ASR3	Area select register 3	W	0 0 0 0 0 0 0 0 _B
0615 _H				0 0 0 0 0 0 1 1 _B
0616 _H	AMR3	Area mask register 3	W	0 0 0 0 0 0 0 0 _B
0617 _H				0 0 0 0 0 0 0 0 _B
0618 _H	ASR4	Area select register 4	W	0 0 0 0 0 0 0 0 _B
0619 _H				0 0 0 0 0 1 0 0 _B
061A _H	AMR4	Area mask register 4	W	0 0 0 0 0 0 0 0 _B
061B _H				0 0 0 0 0 0 0 0 _B
061C _H	ASR5	Area select register 5	W	0 0 0 0 0 0 0 0 _B
061D _H				0 0 0 0 0 1 0 1 _B
061E _H	AMR5	Area mask register 5	W	0 0 0 0 0 0 0 0 _B
061F _H				0 0 0 0 0 0 0 0 _B
0620 _H	AMD0	Area mode register 0	R/W	— — — 0 0 1 1 1 _B
0621 _H	AMD1	Area mode register 1	R/W	0 — — 0 0 0 0 0 _B
0622 _H	AMD32	Area mode register 32	R/W	0 0 0 0 0 0 0 0 _B
0623 _H	AMD4	Area mode register 4	R/W	0 — — 0 0 0 0 0 _B
0624 _H	AMD5	Area mode register 5	R/W	0 — — 0 0 0 0 0 _B
0625 _H	DSCR	DRAM signal control register	W	0 0 0 0 0 0 0 0 _B
0626 _H	RFCR	Refresh control register	R/W	— — X X X X X X _B
0627 _H				0 0 — — — 0 0 0 _B
0628 _H	EPCR0	External pin control register 0	W	— 1 0 0 1 1 0 0 _B
0629 _H				— 1 1 1 1 1 1 1 _B
062A _H	EPCR1	External pin control register 1	W	— — — — — — — _B
062B _H				1 1 1 1 1 1 1 1 _B
062C _H	DMCR4	DRAM control register 4	R/W	0 0 0 0 0 0 0 0 _B
062D _H				0 0 0 0 0 0 0 — _B
062E _H	DMCR5	DRAM control register 5	R/W	0 0 0 0 0 0 0 0 _B
062F _H				0 0 0 0 0 0 0 — _B
0630 _H to 07FD _H	Vacant			

(Continued)

MB91103 Series

(Continued)

Address	Register name (Abbreviated)	Register name	Read/write	Initial value
07FE _H	LER	Little endian register	W	-----000 _B
07FF _H	MODR	Mode register	W	XXXXXXXX _B

Note: Do not use vacant areas.

■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level *1		Interrupt vector *2	
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Vector address
Reset *1	0	00	—	—	3FC _H	000FFFFC _H
Reserved for system	1	01	—	—	3F8 _H	000FFFF8 _H
Reserved for system	2	02	—	—	3F4 _H	000FFFF4 _H
Reserved for system	3	03	—	—	3F0 _H	000FFFF0 _H
Reserved for system	4	04	—	—	3EC _H	000FFFE _C
Reserved for system	5	05	—	—	3E8 _H	000FFFE8 _H
Reserved for system	6	06	—	—	3E4 _H	000FFFE4 _H
Co-processor unattended trap	7	07	—	—	3E0 _H	000FFFE0 _H
Co-processor error trap	8	08	—	—	3DC _H	000FFFD _C
INTE instruction	9	09	Fixed to 4	—	3D8 _H	000FFFD8 _H
Instruction break exception	10	0A	—	—	3D4 _H	000FFFD4 _H
Operand break trap	11	0B	—	—	3D0 _H	000FFFD0 _H
Step trace trap	12	0C	Fixed to 4	—	3CC _H	000FFFC _C
Reserved for system	13	0D	—	—	3C8 _H	000FFFC8 _H
Exception for undefined instruction	14	0E	—	—	3C4 _H	000FFFC4 _H
NMI (user) request	15	0F	Fixed to 15 (F _H)	—	3C0 _H	000FFFC0 _H
Parity error area 4	16	10	ICR00	00000400 _H	3BC _H	000FFFB _C
Parity error area 5	17	11	ICR01	00000401 _H	3B8 _H	000FFFB8 _H
External interrupt 0	18	12	ICR02	00000402 _H	3B4 _H	000FFFB4 _H
External interrupt 1	19	13	ICR03	00000403 _H	3B0 _H	000FFFB0 _H
External interrupt 2	20	14	ICR04	00000404 _H	3AC _H	000FFFA _C
External interrupt 3	21	15	ICR05	00000405 _H	3A8 _H	000FFFA8 _H
External interrupt 4	22	16	ICR06	00000406 _H	3A4 _H	000FFFA4 _H
External interrupt 5	23	17	ICR07	00000407 _H	3A0 _H	000FFFA0 _H
External interrupt 6	24	18	ICR08	00000408 _H	39C _H	000FFF9 _C

(Continued)

MB91103 Series

Interrupt causes	Interrupt number		Interrupt level *1		Interrupt vector *2	
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Vector address
External interrupt 7	25	19	ICR09	00000409 _H	398 _H	000FFF98 _H
Reserved for system	26	1A	ICR10	0000040A _H	394 _H	000FFF94 _H
UART0 receive complete	27	1B	ICR11	0000040B _H	390 _H	000FFF90 _H
UART1 receive complete	28	1C	ICR12	0000040C _H	38C _H	000FFF8C _H
Reserved for system	29	1D	ICR13	0000040D _H	388 _H	000FFF88 _H
UART0 transmit complete	30	1E	ICR14	0000040E _H	384 _H	000FFF84 _H
UART1 transmit complete	31	1F	ICR15	0000040F _H	380 _H	000FFF80 _H
Reserved for system	32	20	ICR16	00000410 _H	37C _H	000FFF7C _H
DMAC0 (complete, error)	33	21	ICR17	00000411 _H	378 _H	000FFF78 _H
DMAC1 (complete, error)	34	22	ICR18	00000412 _H	374 _H	000FFF74 _H
Reserved for system	35	23	ICR19	00000413 _H	370 _H	000FFF70 _H
Reserved for system	36	24	ICR20	00000414 _H	36C _H	000FFF6C _H
DMAC4 (complete, error)	37	25	ICR21	00000415 _H	368 _H	000FFF68 _H
DMAC5 (complete, error)	38	26	ICR22	00000416 _H	364 _H	000FFF64 _H
DMAC6 (complete, error)	39	27	ICR23	00000417 _H	360 _H	000FFF60 _H
Reserved for system	40	28	ICR24	00000418 _H	35C _H	000FFF5C _H
A/D (successive approximation type)	41	29	ICR25	00000419 _H	358 _H	000FFF58 _H
Reload timer 0	42	2A	ICR26	0000041A _H	354 _H	000FFF54 _H
Reload timer 1	43	2B	ICR27	0000041D _H	350 _H	000FFF50 _H
U/D counter 0	44	2C	ICR28	0000041C _H	34C _H	000FFF4C _H
U/D counter 1	45	2D	ICR29	0000041D _H	348 _H	000FFF48 _H
ICU0	46	2E	ICR30	0000041E _H	344 _H	000FFF44 _H
ICU1	47	2F	ICR31	0000041F _H	340 _H	000FFF40 _H
ICU2	48	30	ICR32	00000420 _H	33C _H	000FFF3C _H
ICU3	49	31	ICR33	00000421 _H	338 _H	000FFF38 _H
OCU0	50	32	ICR34	00000422 _H	334 _H	000FFF34 _H
OCU1	51	33	ICR35	00000423 _H	330 _H	000FFF30 _H
OCU2	52	34	ICR36	00000424 _H	32C _H	000FFF2C _H
OCU3	53	35	ICR37	00000425 _H	328 _H	000FFF28 _H
OCU4	54	36	ICR38	00000426 _H	324 _H	000FFF24 _H
OCU5	55	37	ICR39	00000427 _H	320 _H	000FFF20 _H

(Continued)

MB91103 Series

(Continued)

Interrupt causes	Interrupt number		Interrupt level *1		Interrupt vector *2	
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Vector address
OCU6	56	38	ICR40	00000428 _H	31C _H	000FFF1C _H
OCU7	57	39	ICR41	00000429 _H	318 _H	000FFF18 _H
U-TIMER 0	58	3A	ICR42	0000042A _H	314 _H	000FFF14 _H
U-TIMER 1	59	3B	ICR43	0000042B _H	310 _H	000FFF10 _H
Reserved for system	60	3C	ICR44	0000042C _H	30C _H	000FFF0C _H
I/O extended serial	61	3D	ICR45	0000042D _H	308 _H	000FFF08 _H
16-bit free-run timer	62	3E	ICR46	0000042E _H	304 _H	000FFF04 _H
Delayed interrupt cause bit	63	3F	ICR47	0000042F _H	300 _H	000FFF00 _H
Reserved for system (used in REALOS *2)	64	40	—	—	2FC _H	000FFEFC _H
Reserved for system (used in REALOS *2)	65	41	—	—	2F8 _H	000FFE8 _H
Used in INT instructions	66 to 255	42 to FF	—	—	2F4 _H to 000 _H	000FFE4 _H to 000FFD00 _H

*1: ICR sets an interrupt level corresponding to the interrupt request into a register provided in the interrupt controller. ICR is provided for each interrupt request.

*2: Vector addresses are given by adding an offset value corresponding to each EIT (exception/interrupt/trap) cause to the TBR value.

TBR (Table Base Register) holds the top address of EIT vector table. Default value (Initial value upon reset 000FFC00_H) is used in "■ Interrupt causes, interrupt vectors and interrupt control register allocations."

MB91103 Series

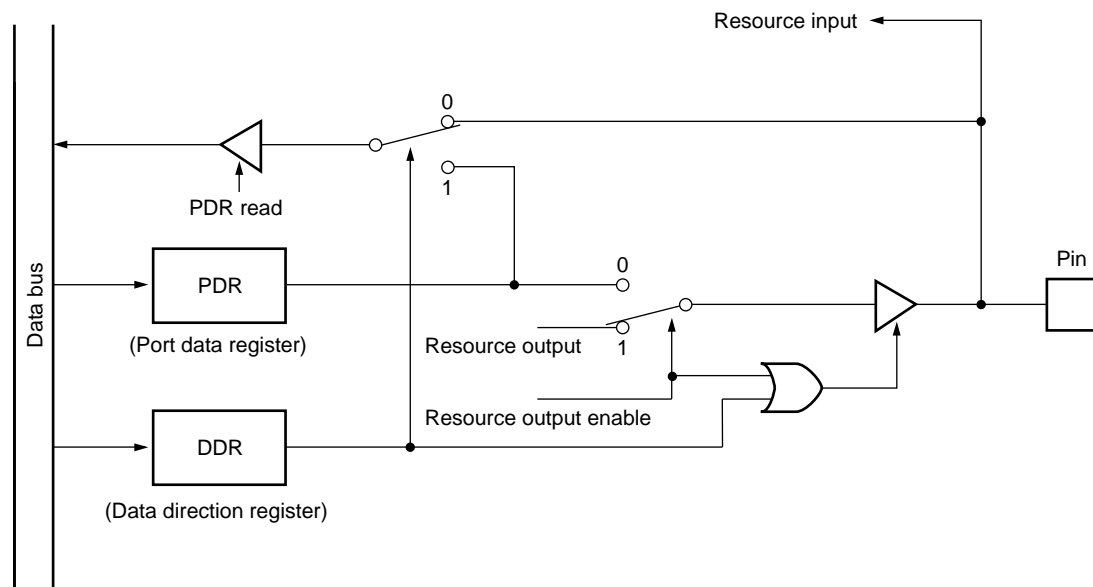
■ PERIPHERAL RESOURCES

1. I/O Ports

There are 2 types of I/O port register structure — port data register (PDR0 to PDRI) and data direction register (DDR0 to DDRI, AIC), where bits PDR0 to PDR I and bits DDR0 to DDRI corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit “0” specifies input and “1” specifies output.

- For input (DDR = “0”) setting;
 - PDR reading operation: reads level of corresponding external pin
 - PDR writing operation: writes set value to PDR
- For output (DDR = “1”) setting;
 - PDR reading operation: reads PDR value
 - PDR writing operation: outputs PDR value to corresponding external pin

• Block diagram



MB91103 Series

• Port data register

Address	bit 7	bit 0	Initial value
000003H	PDR0		XXXXXXXX _B (R/W)
000002H	PDR1		XXXXXXXX _B (R/W)
000001H	PDR2		XXXXXXXX _B (R/W)
000005H	PDR6		XXXXXXXX _B (R/W)
00000BH	PDR8		XXX- - XXX _B (R/W)
00000AH	PDR9		- - XXXXXX _B (R/W)
000009H	PDRA		- XXXXXX _B (R/W)
000008H	PDRB		XXXXXXXX _B (R/W)
000011H	PDRD		XXXXXXXX _B (R/W)
000012H	PDRE		XXXXXXXX _B (R/W)
000013H	PDRF		XXXXXXXX _B (R/W)
000014H	PDRG		XXXXXXXX _B (R/W)
000015H	PDRH		XXXXXXXX _B (R/W)
000016H	PDRI		- - - - XXXX _B (R/W)

• Data direction register

Address	bit 7	bit 0	Initial value
000603H	DDR0		00000000 _B (W)
000602H	DDR1		00000000 _B (W)
000601H	DDR2		00000000 _B (W)
000605H	DDR6		00000000 _B (W)
00060BH	DDR8		000- - 000 _B (W)
00060AH	DDR9		- - 000000 _B (W)
000609H	DDRA		- 0000000 _B (W)
000608H	DDRB		00000000 _B (W)
0000D1H	DDRD		00000000 _B (W)
0000D2H	DDRE		00000000 _B (W)
0000D3H	DDRF		00000000 _B (W)
0000D4H	DDRG		00000000 _B (W)
0000D5H	DDRH		00000000 _B (W)
0000D6H	DDRI		- - - - 0000 _B (W)
0000D7H	AIC*		00000000 _B (W)

Access type(s) in parenthesis

R/W : Read and write access type

W : Write only

- : Vacant

X : Not fixed

* : A/D converter input/general-purpose input port selective by port D input

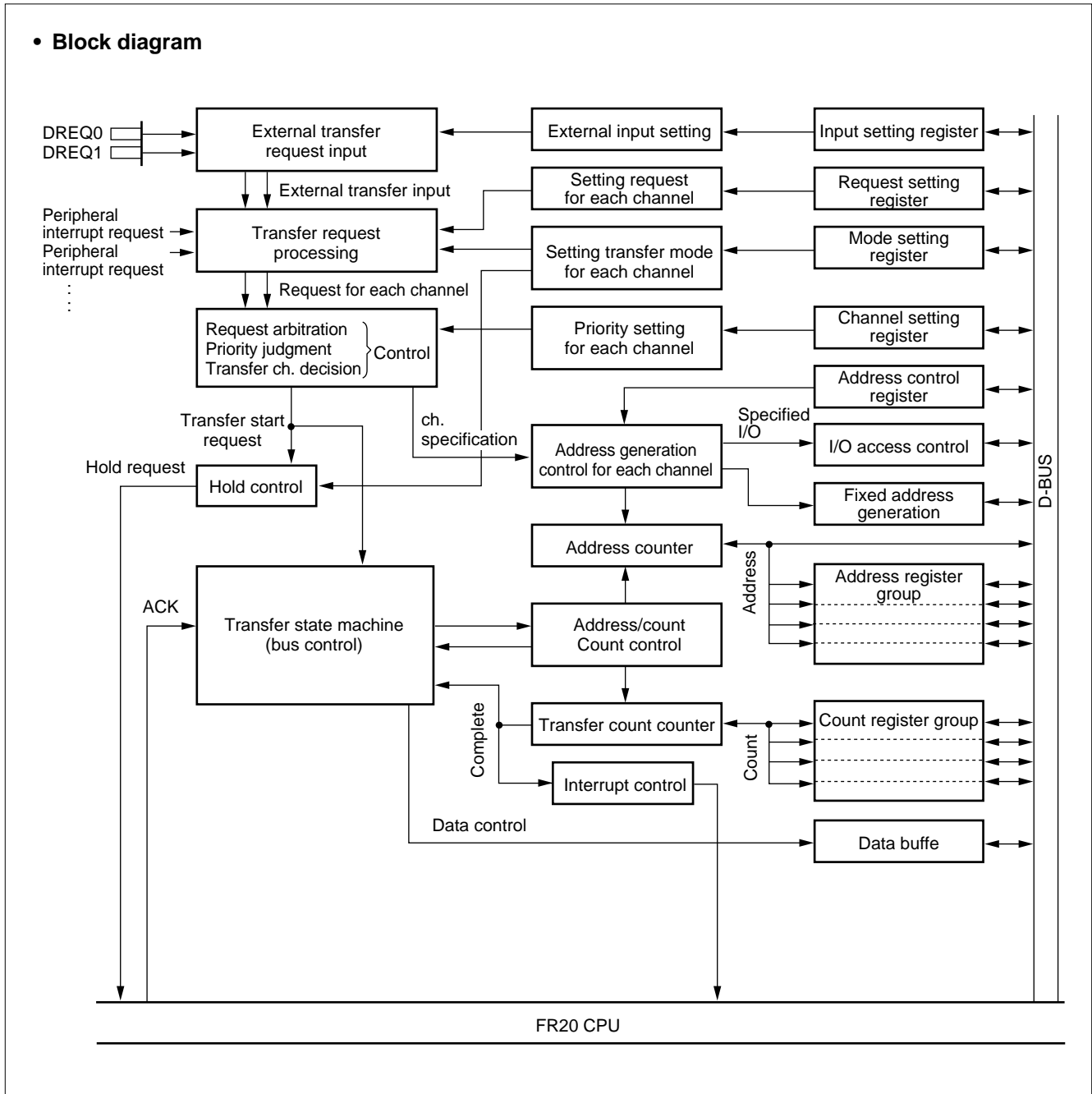
MB91103 Series

2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR 20 series devices, and performs DMA (Direct Memory Access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

• Block diagram

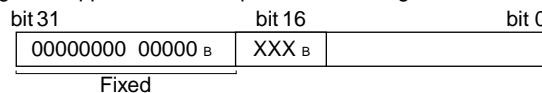


MB91103 Series

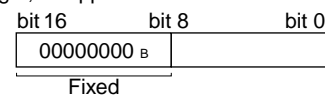
• Registers

Address	bit 31	bit 16	bit 0	Access
00000200 _H	DMACS0			R/W
00000204 _H	DMACC0			R/W
00000208 _H	DMACS1			R/W
0000020C _H	DMACC1			R/W
00000220 _H	DMACS4			R/W
00000224 _H	DMACC4			R/W
00000228 _H	DMACS5			R/W
0000022C _H	DMACC5			R/W
00000230 _H	DMACS6			R/W
00000234 _H	DMACC6			R/W
00000240 _H	DMAAR0			R/W
00000244 _H	DMAAR1			R/W
00000248 _H	DMAAR2 *1			R/W
0000024C _H	DMAAR3 *1			R/W
00000250 _H	DMAAR4 *1			R/W
00000254 _H	DMAAR5 *1			R/W
00000258 _H	DMAAR6 *1			R/W
0000025C _H	DMAAR7 *1			R/W
00000260 _H	DMACT0			R/W
00000262 _H		DMACT1		R/W
00000268 _H	DMACT4 *2			R/W
0000026A _H		DMACT5 *3		R/W
0000026C _H	DMACT6 *2			R/W
00000274 _H	DMACR *1			R/W

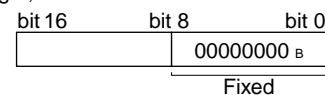
*1: 32-bit length, fix upper 16 bits except for the least-significant 3 bits to "0".



*2: 16-bit length, fix upper 8 bits to "0".



*3: 16-bit length, fix lower 8 bits to "0".



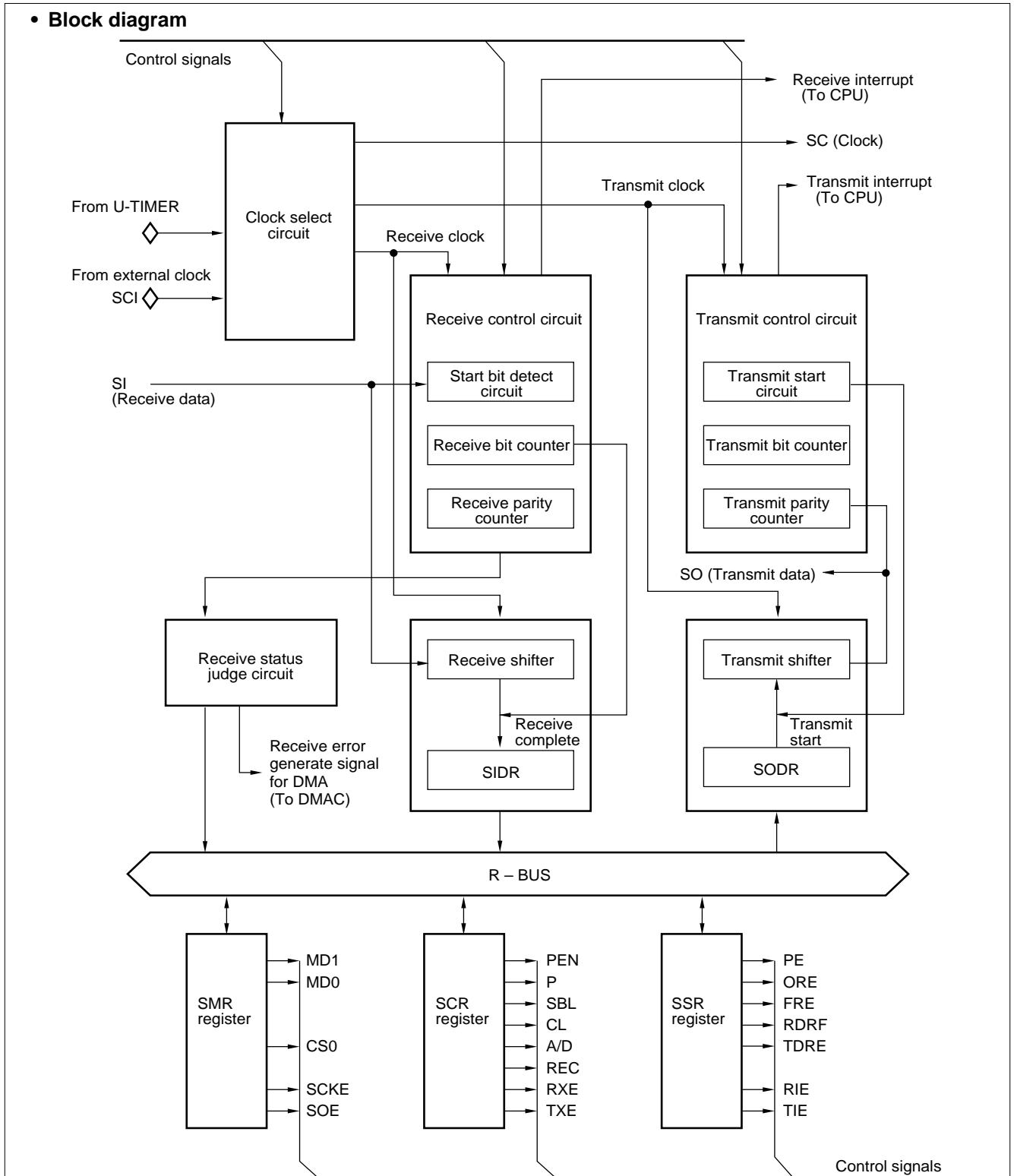
MB91103 Series

3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication.

The MB91103 consists of 2 channels of UART.

• Block diagram



MB91103 Series

• Registers

Address	bit 15	bit 8	bit 0	Initial value
0000001E _H	SCR0			0 0 0 0 0 1 0 0 _B (R/W)
00000022 _H	SCR1			0 0 0 0 0 1 0 0 _B (R/W)
0000001F _H		SMR0		0 0 - - 0 - 0 0 _B (R/W)
00000023 _H		SMR1		0 0 - - 0 - 0 0 _B (R/W)
0000001C _H	SSR0			0 0 0 0 1 - 0 0 _B (R/W)
00000020 _H	SSR1			0 0 0 0 1 - 0 0 _B (R/W)
0000001D _H		SIDR0/SODR0		X X X X X X X X _B (R/W)
00000021 _H		SIDR1/SIDR1		X X X X X X X X _B (R/W)

Access type(s) in parenthesis
 R/W: Read and write access type
 - : Vacant
 X : Not fixed

4. I/O Extended Serial Interface

This block is a serial interface of 8-bit × 1 structure enabling clock synchronous data transfer. Data transfer format of LSB first or MSB first can be selected.

DMA transfer operation is enabled by interrupt request.

There are two serial I/O operating modes.

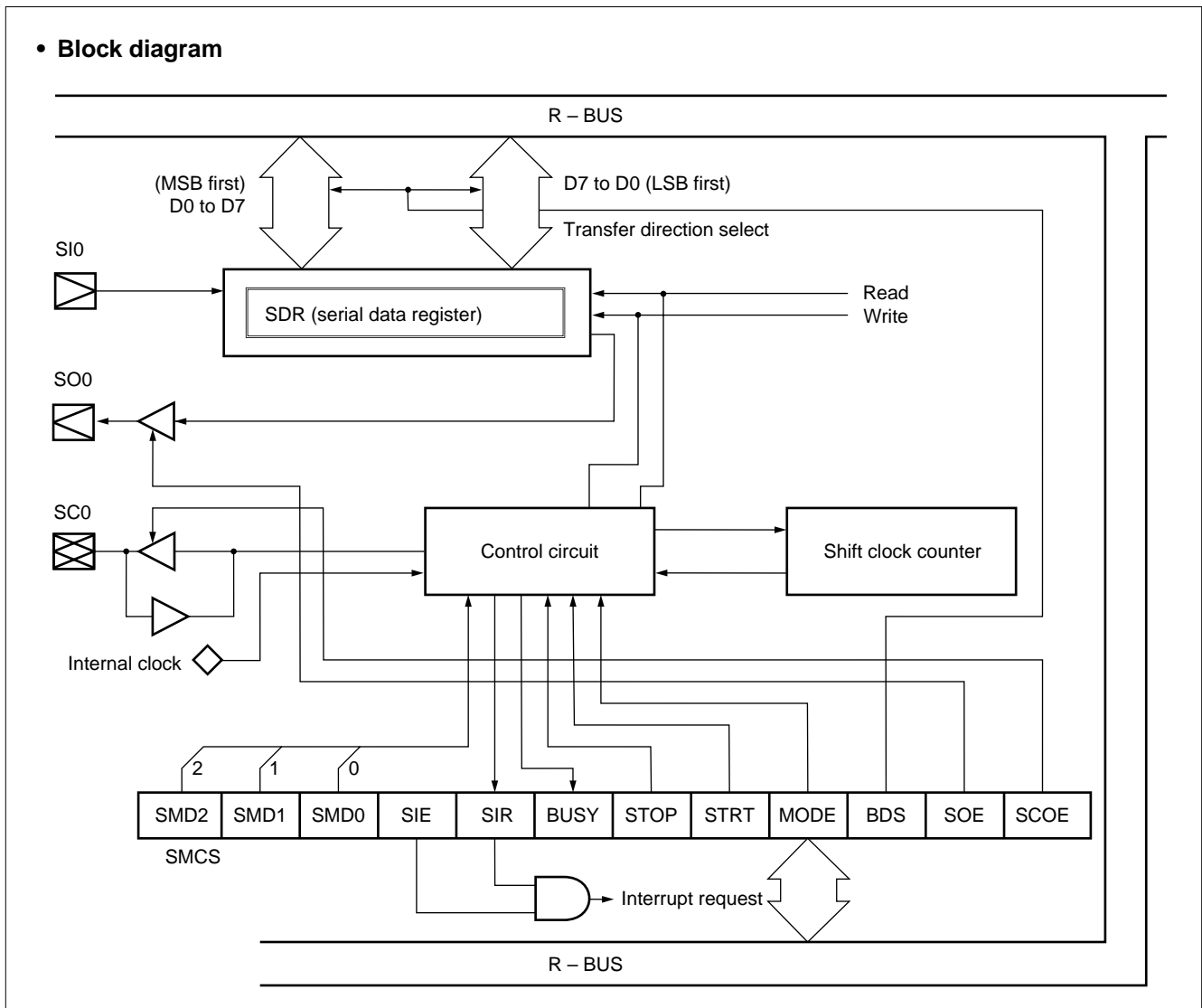
Internal shift clock mode : In this mode, data transfer operation is synchronized with internal clock.

It can be selected from 10/20/80/160/320 frequency division of machine clock.

External shift clock mode : In this mode, data transfer operation is synchronized with clock input from external pin (SC0). Data transfer by CPU instructions is enabled when the general port sharing the external pin (SC0) is so configured.

MB91103 Series

• Block diagram



• Registers

Address	bit 15	bit 8	bit 0	Initial value
0000001Ah	SMCS			0 0 0 0 0 1 0 _B (R/W) - - - - 0 0 0 0 _B (R/W)
00000019h	SDR			X X X X X X X _B (R/W)

Access type(s) in parenthesis
 R/W : Read and write access type
 - : Vacant
 X : Not fixed

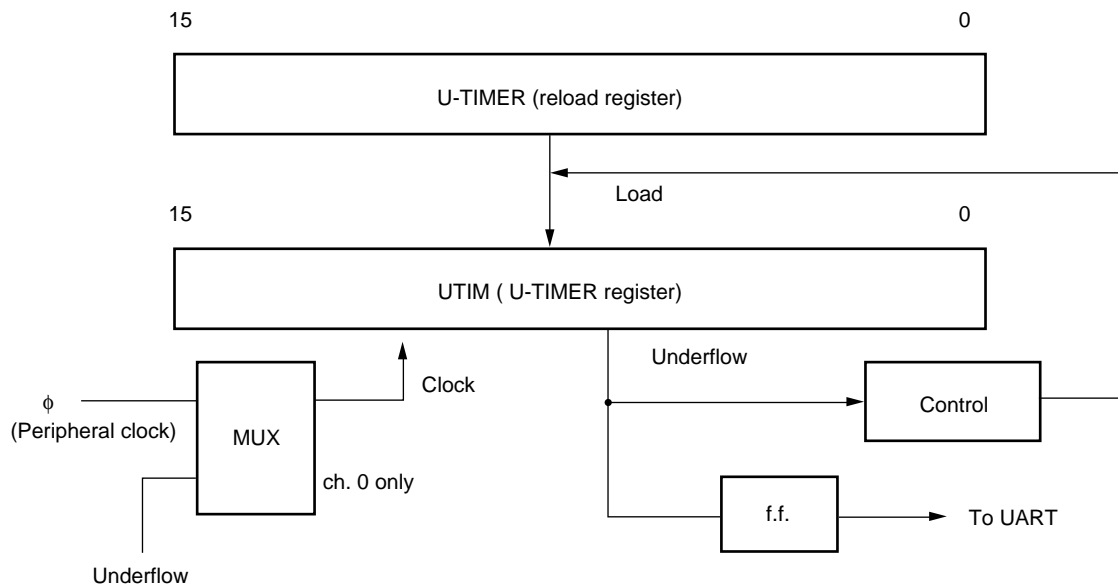
5. U-TIMER (16-bit timer for UART baud rate generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91103 has 2 channel U-TIMER embedded on the chip. By combining 2 interval timers in cascade, an interval of up to $2^{32} \times \phi$ can be counted.

• Block diagram



• Registers

Address	bit 15	bit 0	Initial value	
00000078 _H	UTIM0/UTIMR0		0 0 0 0 0 0 0 0 _B	(R/W)
0000007C _H	UTIM1/UTIMR1		0 0 0 0 0 0 0 0 _B	(R/W)
0000007B _H	UTIMC0		0 - - 0 0 0 0 1 _B	(R/W)
0000007F _H	UTIMC1		0 - - 0 0 0 0 1 _B	(R/W)

Access type(s) in parenthesis
 R/W: Read and write access type
 - : Vacant
 X : Not fixed

MB91103 Series

6. 16-bit Reload Timer

The 16-bit timer consists of a 16-bit down counter, a 16-bit reload timer, a pre-scaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock) or external clock.

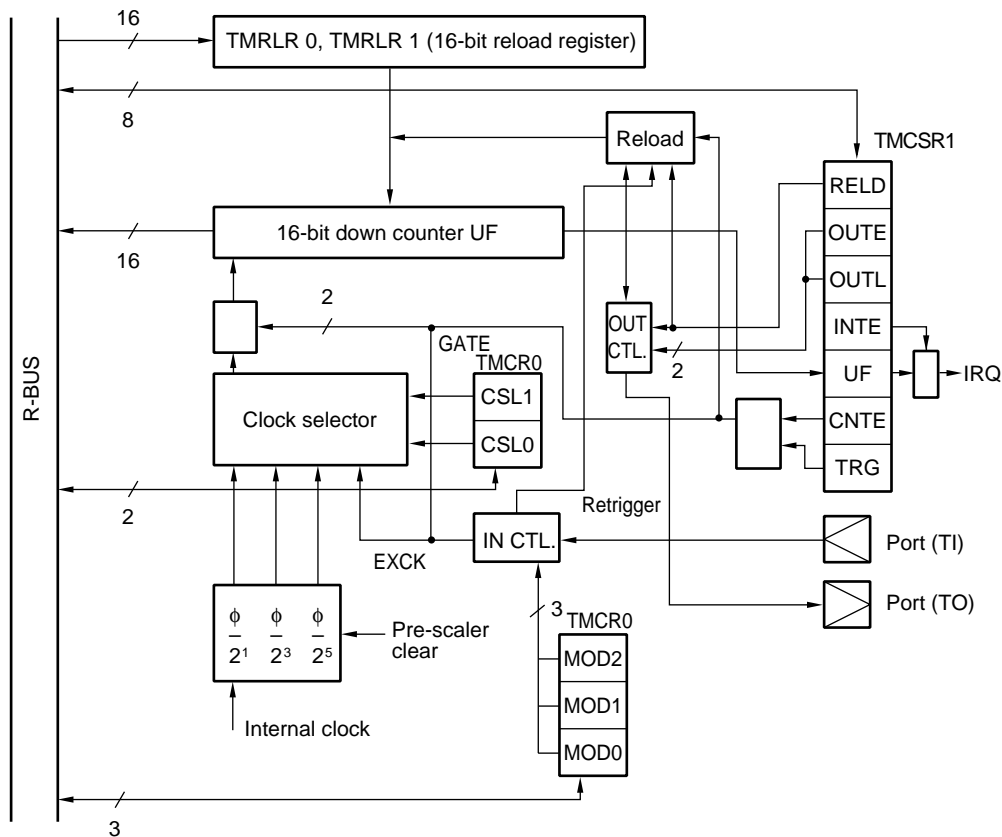
The input/output pin (TO) outputs a deleted toggle wave on every underflow in the reload mode and outputs a square wave indicating the timer is in counting operation in the one-shot mode.

The input pin (TI) is configured as an event input in the event count mode, a trigger input in the internal clock mode and also operates as a gate input.

The external event count function in the reload mode can operate as a external clock divider.

The MB91103 consists of 2 channels of 16-bit reload timer.

• Block diagram



MB91103 Series

• Registers

Address	bit 15	bit 0	Initial value	
0000002E _H	TMCSR0		- - - 0 0 0 0 _B 0 0 0 0 0 0 0 0 _B	(R/W)
00000036 _H	TMCSR1		- - - 0 0 0 0 _B 0 0 0 0 0 0 0 0 _B	(R/W)
0000002A _H	TMR0		X X X X X X X X _B X X X X X X X X _B	(R)
00000032 _H	TMR1		X X X X X X X X _B X X X X X X X X _B	(R)
00000028 _H	TMRLR0		X X X X X X X X _B X X X X X X X X _B	(W)
00000030 _H	TMRLR1		X X X X X X X X _B X X X X X X X X _B	(W)

Access type(s) in parenthesis

R/W : Read and write type

R : Read only

W : Write only

- : Vacant

X : Not fixed

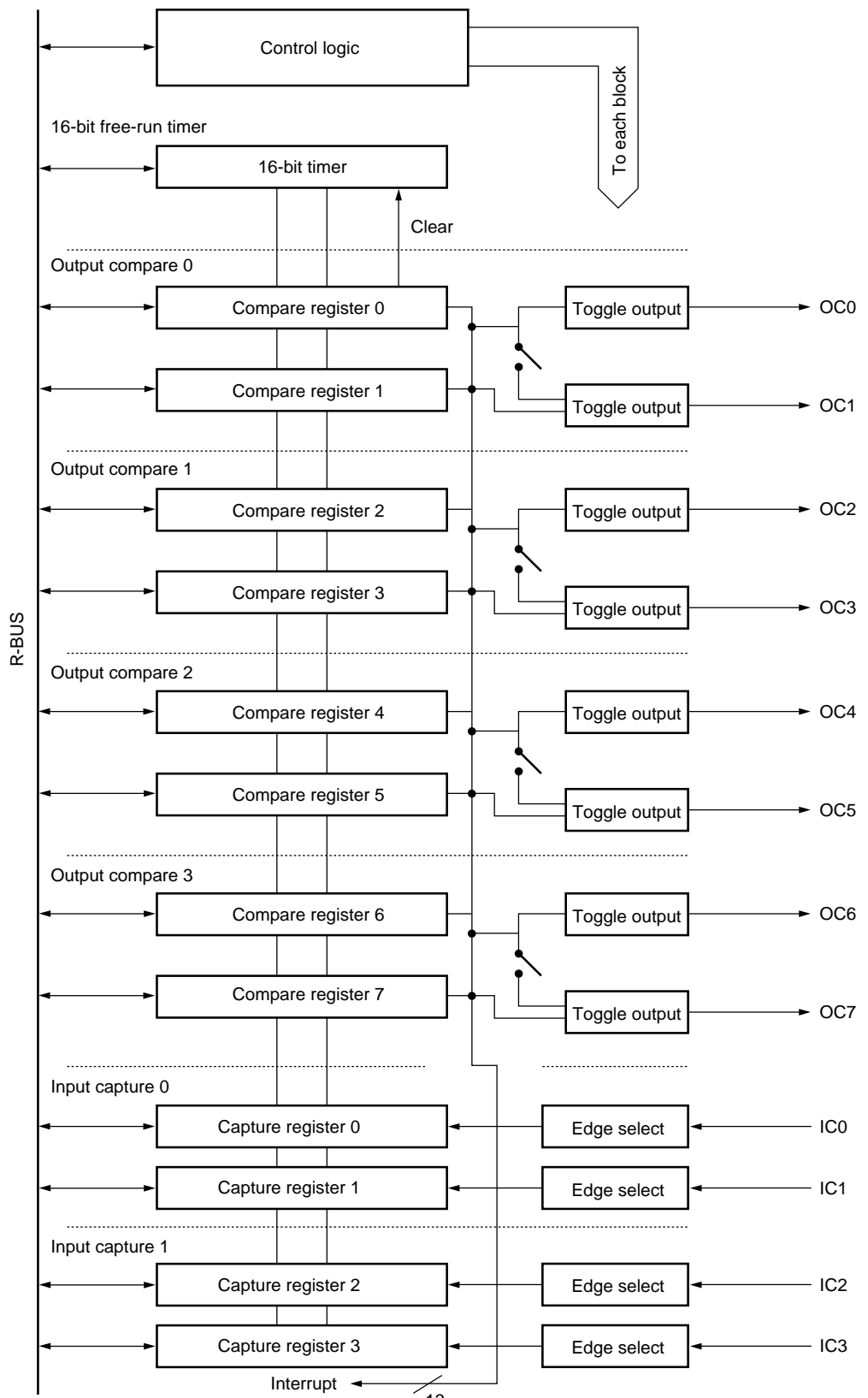
7. Real Time Input/Output Timer

The 16-bit input/output timer consists of a 16-bit free-run timer, 8 output compares and 4 input capture modules.

By using these functions, 8 independent wave outputs based on the 16-bit free-run timer as well as input pulse width measurement and external clock cycle measurement can be realized.

MB91103 Series

• Block diagram



MB91103 Series

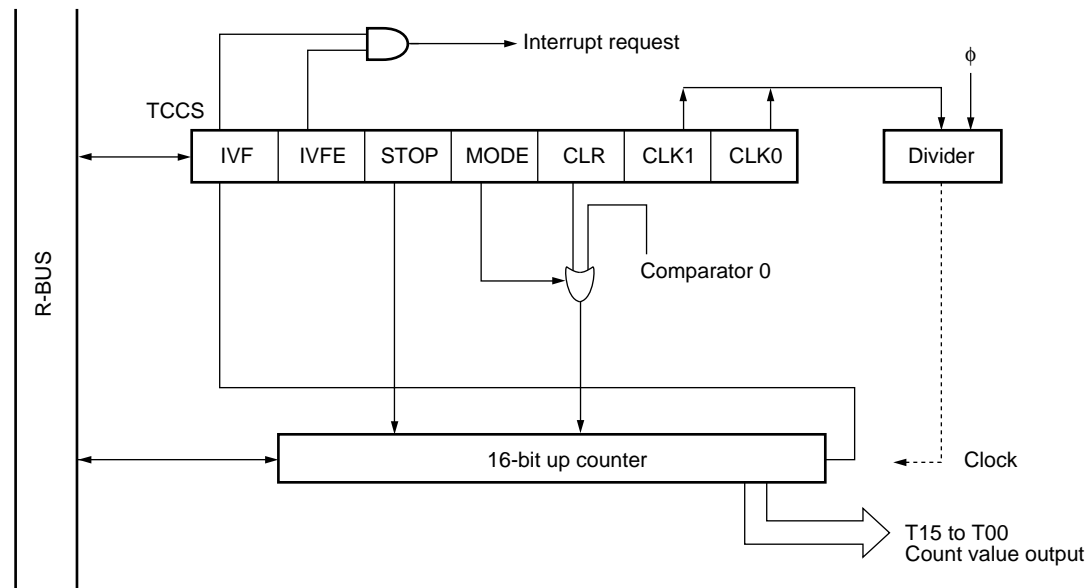
(1) 16-bit Free-Run Timer

The 16-bit free-run timer consists of a 16-bit up/down counter and a control status register.

Count value of this timer is used in output compare and input capture blocks as a basic time.

- Count clock can be selected from 4 types of frequencies ($\phi/4$, $\phi/16$, $\phi/32$, $\phi/64$).
- Interrupt can be issued upon count overflow.
- Selecting a mode and setting the count value as equaling to the value of compare register "0" initializes the counter.

• Block diagram



• Registers

Address	bit 15	bit 8	bit 0	Initial value	
00000074 _H	TCDT			00000000 _B 00000000 _B	(R/W)
00000077 _H	TCCS			00000000 _B	(R/W)

Access type(s) in parenthesis
R/W: Read and write access type

MB91103 Series

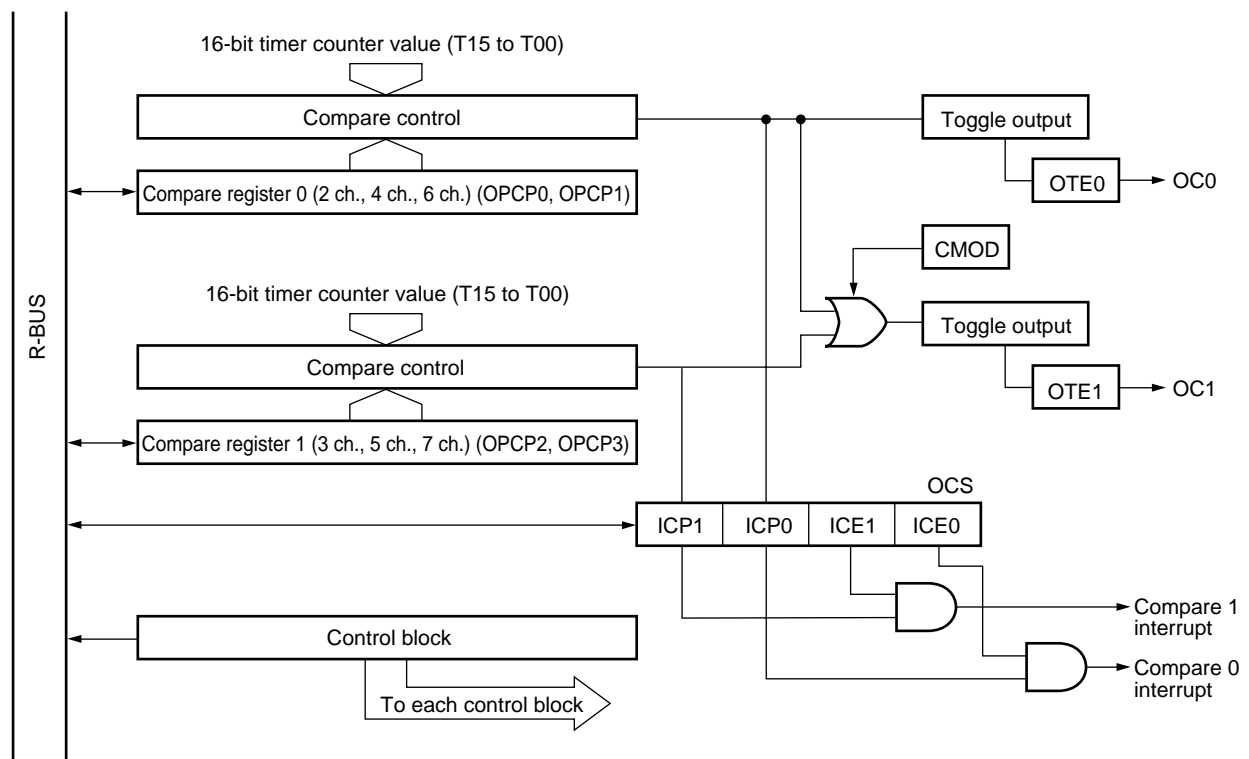
(2) Output Compare

The output compare consists of a 16-bit compare register, compare output pin block and a control register.

When the value set in the compare register matches with the 16-bit free-run timer value, output level is reversed, enabling an interrupt request to be issued.

- 8 compare registers can operate independently. A pair of compare registers can be used for controlling output pin levels.
- Initial output level of output pins can be specified.
- An interrupt is issued when compare value matches with timer value.

• Block diagram



Combinations of compare register 0 and 1: ch.0, ch.1/ch.2, ch.3/ch.4, ch.5/ch.6, ch.7

MB91103 Series

• Registers

Address	bit 15	bit 0	Initial value	
00000058H	OPCP0		XXXXXXXX B XXXXXXXX B	(R/W)
0000005AH	OPCP1		XXXXXXXX B XXXXXXXX B	(R/W)
00000060H	OPCP2		XXXXXXXX B XXXXXXXX B	(R/W)
00000062H	OPCP3		XXXXXXXX B XXXXXXXX B	(R/W)
00000068H	OPCP4		XXXXXXXX B XXXXXXXX B	(R/W)
0000006AH	OPCP5		XXXXXXXX B XXXXXXXX B	(R/W)
00000070H	OPCP6		XXXXXXXX B XXXXXXXX B	(R/W)
00000072H	OPCP7		XXXXXXXX B XXXXXXXX B	(R/W)
00000054H	OCS0		- - - 0000 B 0000 - - 00 B	(R/W)
0000005CH	OCS1		- - - 0000 B 0000 - - 00 B	(R/W)
00000064H	OCS2		- - - 0000 B 0000 - - 00 B	(R/W)
0000006CH	OCS1		- - - 0000 B 0000 - - 00 B	(R/W)

Access type(s) in parenthesis
 R/W : Read and write access type
 - : Vacant
 X : Not fixed

MB91103 Series

(3) Input Capture

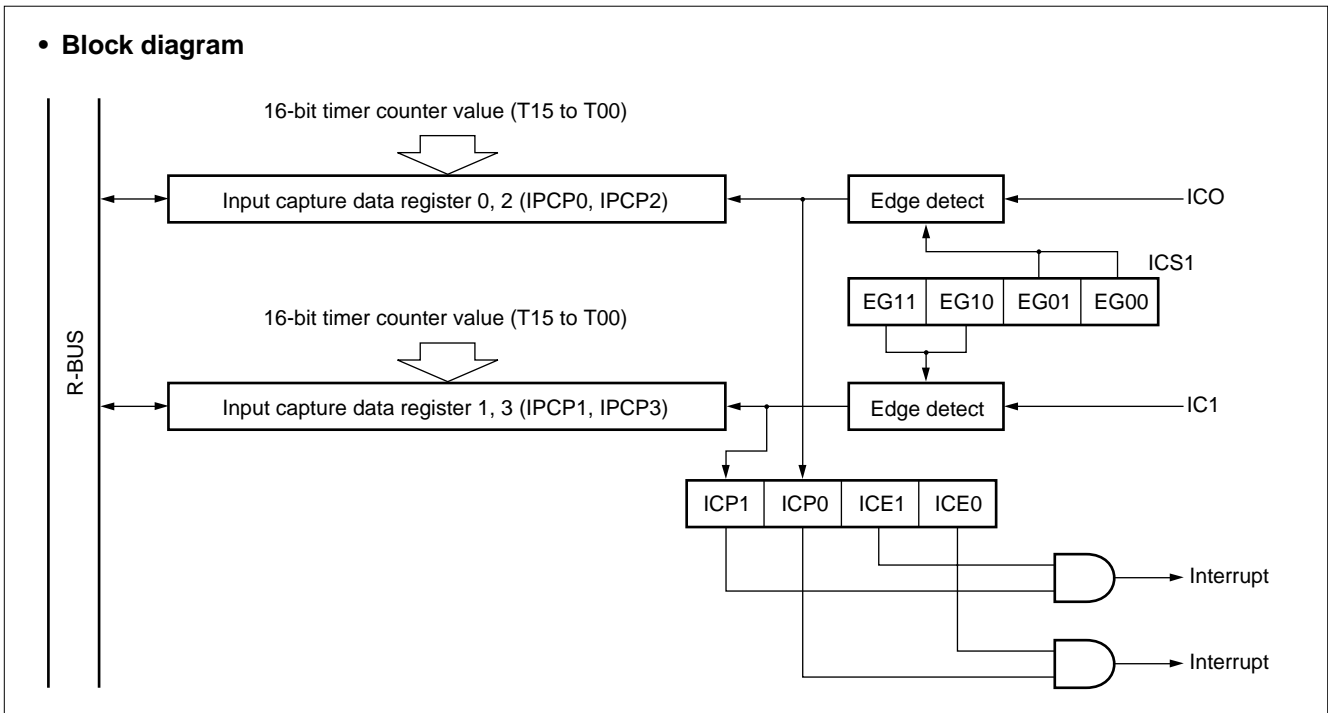
The input capture consists of input capture data registers and input capture control status registers.

The input capture detects a rising edge, a falling edge or both edges of external input signal and hold the 16-bit free-run timer value at the moment into the register. The input capture can issue an interrupt upon edge detection, if enabled.

Every input capture has a corresponding output pin.

- Effective edge of external input can be selected from rising, falling or both edges.
- The input capture issues an interrupt upon detection of an effective edge, if enabled.

• Block diagram



• Registers

Address	bit 15	bit 8	bit 0	Initial value	
00000048H	IPCP0			XXXXXXXX B XXXXXXXX B	(R)
0000004AH	IPCP1			XXXXXXXX B XXXXXXXX B	(R)
00000050H	IPCP2			XXXXXXXX B XXXXXXXX B	(R)
00000052H	IPCP3			XXXXXXXX B XXXXXXXX B	(R)
00000045H		ICS0		00000000 B	(R/W)
0000004DH		ICS1		00000000 B	(R/W)

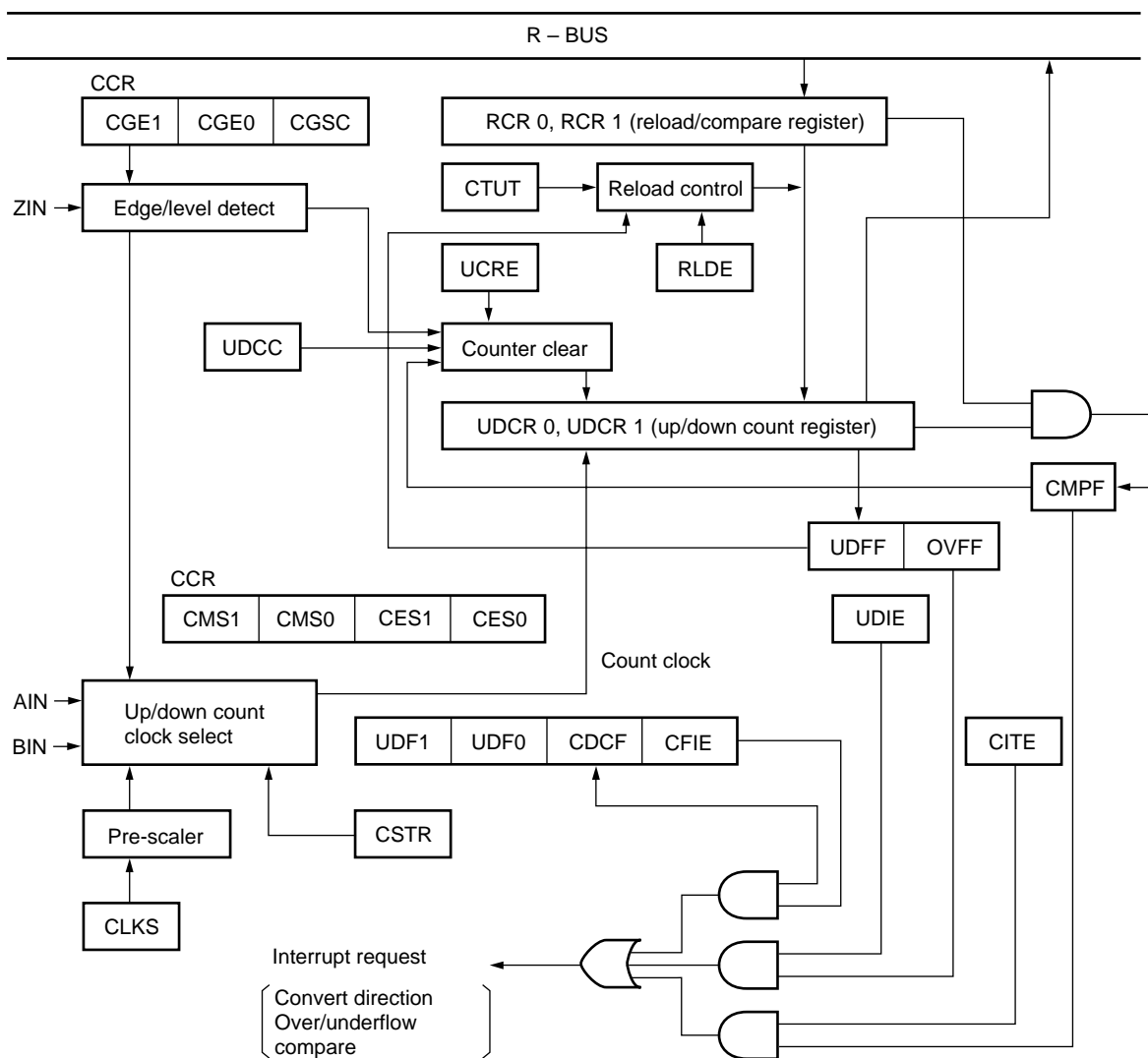
Access type(s) in parenthesis
 R/W: Read and write access type
 R : Read only
 X : Not fixed

8. Up/down Counter

The up/down counter consists of 3 event input pins, a 16-bit up/down counter, 16-bit reload/compare register and peripheral circuits (control/status register) controlling these functions.

The MB91103 consists of 2 channels of counter/timer.

• Block diagram



MB91103 Series

• Registers

Address	bit 15	bit 8	bit 0	Initial value	
00000084 _H	UDCR0			00000000 _B 00000000 _B	(R)
0000008C _H	UDCR1			00000000 _B 00000000 _B	(R)
00000086 _H	RCR0			00000000 _B 00000000 _B	(W)
0000008E _H	RCR1			00000000 _B 00000000 _B	(W)
0000008B _H		CSR0		00000000 _B	(R/W)
00000093 _H		CSR1		00000000 _B	(R/W)
00000088 _H	CCR0			- 0000000 _B - 0001000 _B	(R/W)
00000090 _H	CCR1			- 0000000 _B - 0001000 _B	(R/W)

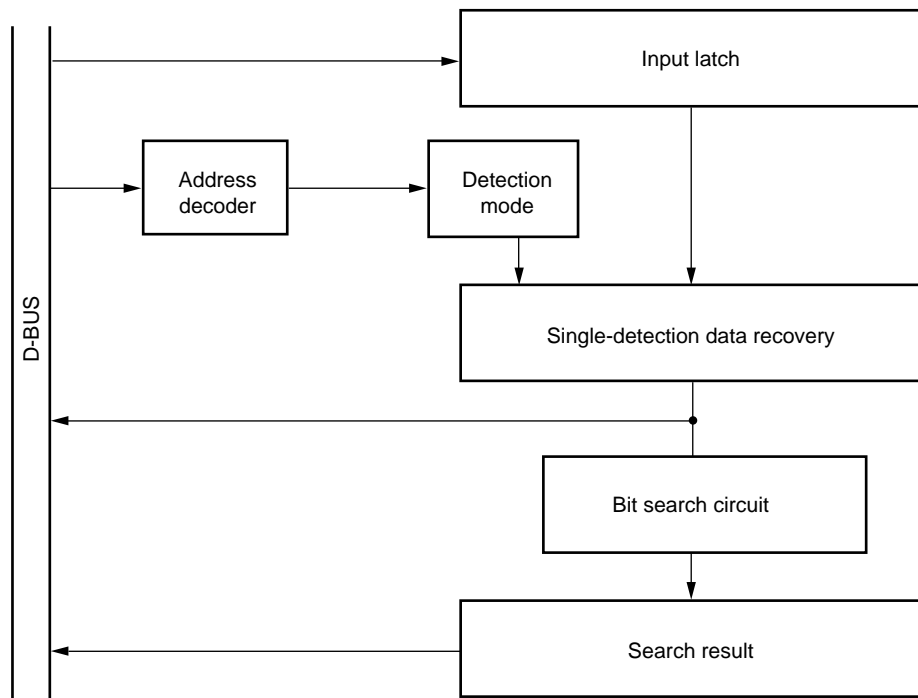
Access type(s) in parenthesis
 R/W : Read and write access type
 R : Read only
 W : Write only
 - : Vacant

MB91103 Series

9. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

• Block diagram



• Registers

Address	bit 31	bit 16	bit 0	Initial value	
000003F0 _H	BSD0			XXXXXXXX XXXXXXXX _B XXXXXXXX XXXXXXXX _B	(W)
000003F4 _H	BSD1			XXXXXXXX XXXXXXXX _B XXXXXXXX XXXXXXXX _B	(R/W)
000003F8 _H	BSDC			XXXXXXXX XXXXXXXX _B XXXXXXXX XXXXXXXX _B	(W)
000003FC _H	BSRR			XXXXXXXX XXXXXXXX _B XXXXXXXX XXXXXXXX _B	(R)

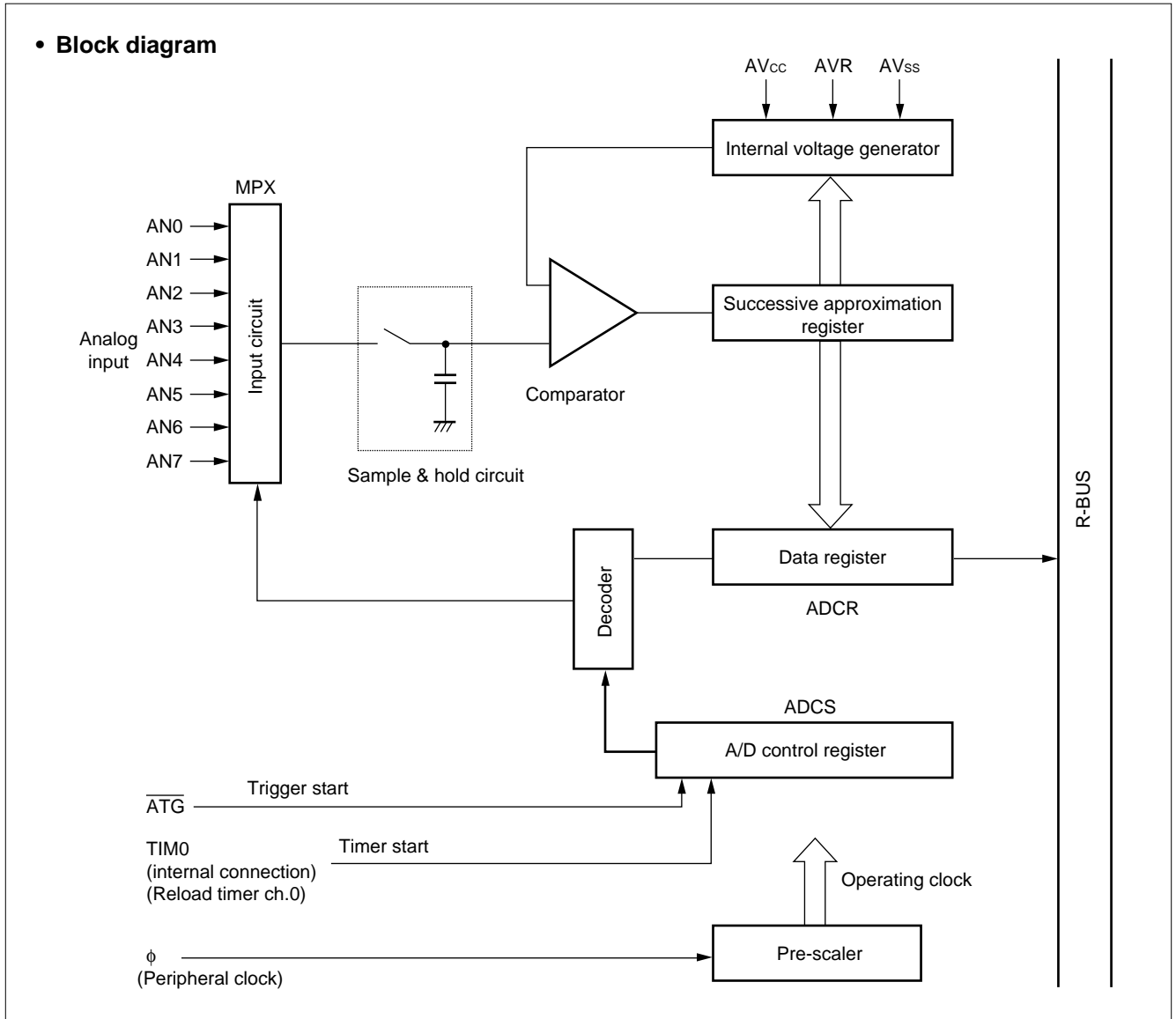
Access type(s) in parenthesis
 R/W : Read and write access type
 R : Read only
 W : Write only

MB91103 Series

10. A/D Converter

The A/D converter converts an analog input voltage to a digital value.

• Block diagram



• Registers

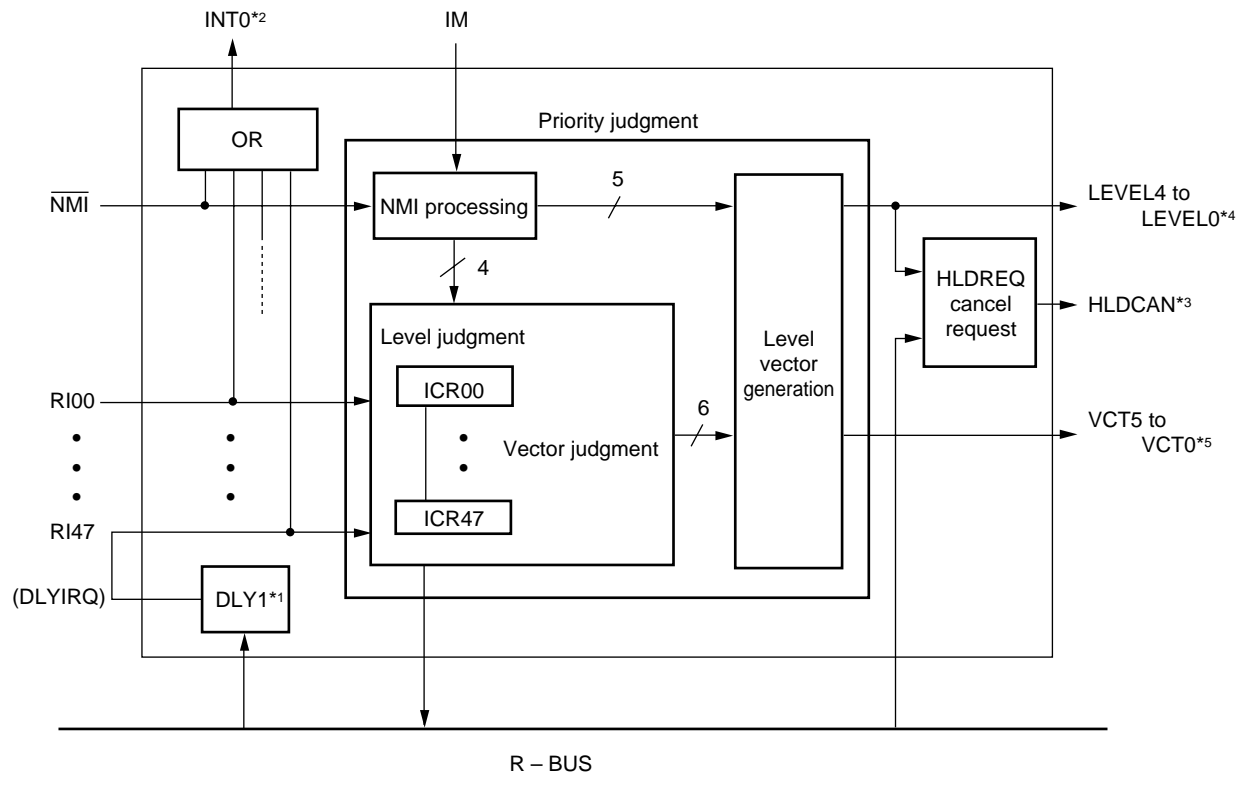
Address	bit 15	bit 0	Initial value	
0000003AH	ADCS		0 0 0 0 0 0 0 0 _B 0 0 0 0 0 0 0 0 _B	(R/W)
00000038H	ADCR		0 0 0 0 0 0 X X _B X X X X X X X X _B	(R)

Access type(s) in parenthesis
 R/W : Read and write access type
 R : Read only
 X : Not fixed

11. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

• Block diagram



*1: DLY1 stands for delayed interrupt module (delayed interrupt generation block).

*2: INT0 is a wake-up signal to clock control block in the sleep or stop status.

*3: HLDREQ is a bus release request signal for bus masters other than CPU.

*4: LEVEL5 to LEVEL0 are interrupt level outputs.

*5: VCT5 to VCT0 are interrupt vector outputs.

MB91103 Series

• Registers

Address	bit 7	bit 0	Initial value	Address	bit 7	bit 0	Initial value
00000400H		ICR00	--- 11111 B (R/W)	0000041AH		ICR26	--- 11111 B (R/W)
00000401H		ICR01	--- 11111 B (R/W)	0000041BH		ICR27	--- 11111 B (R/W)
00000402H		ICR02	--- 11111 B (R/W)	0000041CH		ICR28	--- 11111 B (R/W)
00000403H		ICR03	--- 11111 B (R/W)	0000041DH		ICR29	--- 11111 B (R/W)
00000404H		ICR04	--- 11111 B (R/W)	0000041EH		ICR30	--- 11111 B (R/W)
00000405H		ICR05	--- 11111 B (R/W)	0000041FH		ICR31	--- 11111 B (R/W)
00000406H		ICR06	--- 11111 B (R/W)	00000420H		ICR32	--- 11111 B (R/W)
00000407H		ICR07	--- 11111 B (R/W)	00000421H		ICR33	--- 11111 B (R/W)
00000408H		ICR08	--- 11111 B (R/W)	00000422H		ICR34	--- 11111 B (R/W)
00000409H		ICR09	--- 11111 B (R/W)	00000423H		ICR35	--- 11111 B (R/W)
0000040AH		ICR10	--- 11111 B (R/W)	00000424H		ICR36	--- 11111 B (R/W)
0000040BH		ICR11	--- 11111 B (R/W)	00000425H		ICR37	--- 11111 B (R/W)
0000040CH		ICR12	--- 11111 B (R/W)	00000426H		ICR38	--- 11111 B (R/W)
0000040DH		ICR13	--- 11111 B (R/W)	00000427H		ICR39	--- 11111 B (R/W)
0000040EH		ICR14	--- 11111 B (R/W)	00000428H		ICR40	--- 11111 B (R/W)
0000040FH		ICR15	--- 11111 B (R/W)	00000429H		ICR41	--- 11111 B (R/W)
00000410H		ICR16	--- 11111 B (R/W)	0000042AH		ICR42	--- 11111 B (R/W)
00000411H		ICR17	--- 11111 B (R/W)	0000042BH		ICR43	--- 11111 B (R/W)
00000412H		ICR18	--- 11111 B (R/W)	0000042CH		ICR44	--- 11111 B (R/W)
00000413H		ICR19	--- 11111 B (R/W)	0000042DH		ICR45	--- 11111 B (R/W)
00000414H		ICR20	--- 11111 B (R/W)	0000042EH		ICR46	--- 11111 B (R/W)
00000415H		ICR21	--- 11111 B (R/W)	0000042FH		ICR47	--- 11111 B (R/W)
00000416H		ICR22	--- 11111 B (R/W)	00000431H		HRCL	--- 11111 B (R/W)
00000417H		ICR23	--- 11111 B (R/W)	00000430H		DICR	----- 0 B (R/W)
00000418H		ICR24	--- 11111 B (R/W)				
00000419H		ICR25	--- 11111 B (R/W)				

Access type(s) in parenthesis
 R/W : Read and write access type
 - : Vacant

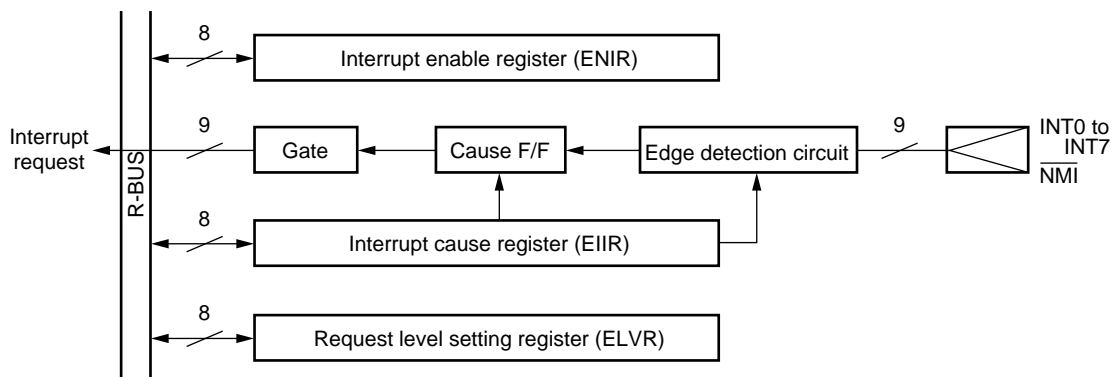
12. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to $\overline{\text{NMI}}$ and INT0 to INT7 pins.

Detecting levels can be selected from "H", "L", rising edge and falling edge (not for $\overline{\text{NMI}}$).

INT1 and INT0 can be used as a DMA request signal.

• Block diagram



• Registers

Address	bit 15	bit 8	bit 0	Initial value	
00000095 _H	ENIR			00000000 _B	(R/W)
00000094 _H	EIRR			00000000 _B	(R/W)
00000098 _H	ELVR			00000000 _B 00000000 _B	(R/W)

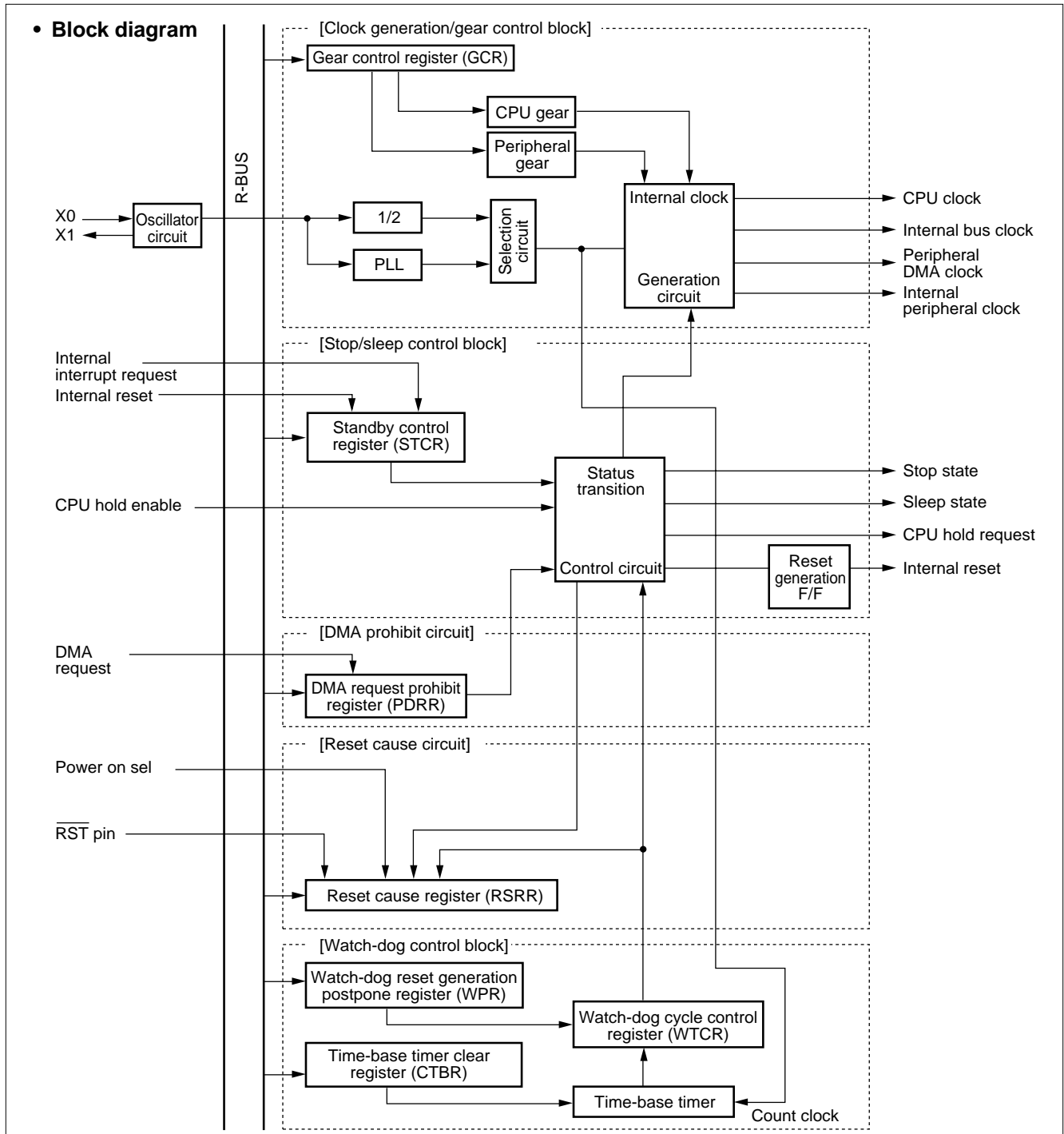
Access type(s) in parenthesis
R/W: Read and write access type

MB91103 Series

13. Clock Generation/control Block

The clock generation/control block consists of the following 6 blocks:

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function
- DMA request prohibit
- PLL (duty ratio adjustment circuit included)



MB91103 Series

• Registers

Address	bit 15	bit 8	bit 0	Initial value	
00000480 _H	RSRR/WTCR			1 - X X X - 0 0 _B	(R/W)
00000481 _H		STCR		0 0 0 1 1 1 - - _B	(R/W)
00000482 _H	PDRR			- - - - 0 0 0 0 _B	(R/W)
00000483 _H		CTBR		X X X X X X X X _B	(W)
00000484 _H	GCR			1 1 - - 1 1 - 1 _B	(R/W)
00000485 _H		WPR		X X X X X X X X _B	(W)

Access type(s) in parenthesis
 R/W : Read and write access type
 W : Write only
 - : Vacant
 X : Not fixed

14. DRAM Controller

The DRAM controller controls interface between CPU and DRAM.

This function is active only when DRME bit of AMD4, AMD5 are set to "1".

The DMCR register also controls parity check functions. This function is active other than the DRAM interface.

• Registers

Address	bit 15	bit 0	Initial value	
0000062C _H	DMCR4		00000000 _B 00000000 - _B	(R/W)
0000062E _H	DMCR5		00000000 _B 00000000 - _B	(R/W)

Access type(s) in parenthesis
 R/W : Read and write access type
 - : Not used

MB91103 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
Analog supply voltage *1	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
Analog reference voltage *1	$AVRH$	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
Analog reference voltage *1	$AVRL$	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
Input voltage *2	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Output voltage *2	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level maximum output current *3	I_{OL}	—	10	mA	
"L" level average output current *4	I_{OLAV}	—	8	mA	
"L" level maximum total output current	ΣI_{OL}	—	100	mA	
"L" level average total output current *5	ΣI_{OLAV}	—	50	mA	
"H" level maximum output current *3	I_{OH}	—	-10	mA	
"H" level average output current *4	I_{OHAV}	—	-4	mA	
"H" level maximum total output current	ΣI_{OH}	—	-50	mA	
"H" level average total output current *5	ΣI_{OHAV}	—	-20	mA	
Power dissipation	P_D	—	990	mW	
Operating temperature	T_A	-10	+70	°C	
Storage temperature	T_{stg}	-55	+150	°C	

*1: Make sure that the voltage does not exceed $V_{CC} + 0.3\text{ V}$.
Make sure AV_{CC} does not exceed V_{CC} when turning on the device.

*2: V_I and V_O must not exceed $V_{CC} + 0.3\text{ V}$.

*3: Maximum output current is a peak current value measured at a corresponding pin.

*4: Average output current is an average current for a 100 ms period at a corresponding pin.

*5: Average total output current is an average current for a 100 ms period for all corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

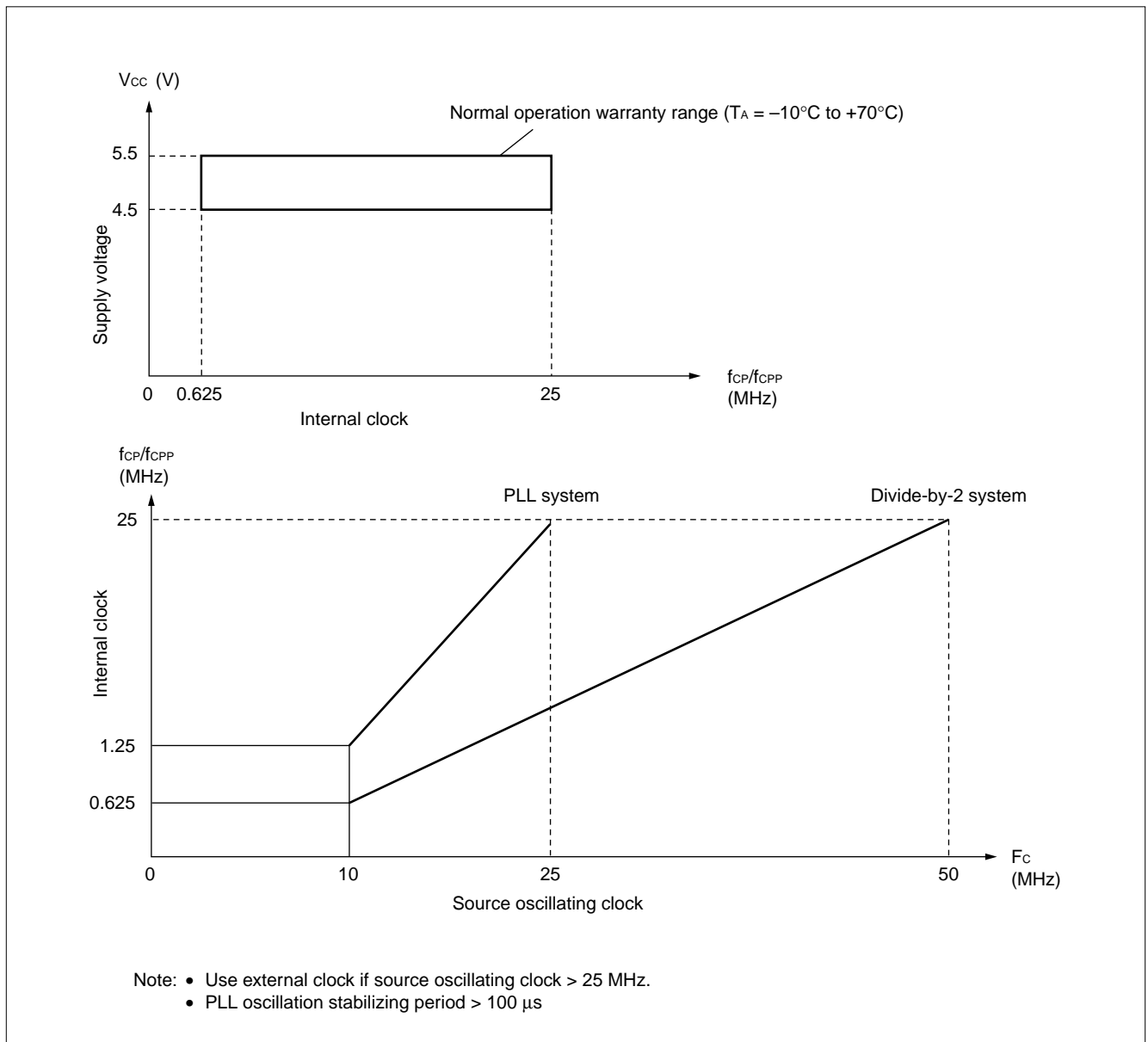
MB91103 Series

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V _{CC}	4.5	5.5	V	Normal operation
		3.0	5.5	V	Retaining the RAM state in stop mode
Analog supply voltage	AV _{CC}	V _{SS} - 0.3	V _{CC} + 0.3	V	
Analog reference voltage	AVRH	AVRL	AV _{CC}	V	
	AVRL	AV _{SS}	AVRH	V	
Operating temperature	T _A	-10	+70	°C	

MB91103 Series



WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB91103 Series

3. DC Characteristics

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	V_{IH}	Input other than following symbols	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	*1	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	V_{IHT}	*2	—	2.2	—	$V_{CC} + 0.3$	V	TTL level
	V_{IHM}	MD0 to MD2	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	V_{IL}	Input other than following symbols	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	V_{ILS}	*1	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	V_{ILT}	*2	—	$V_{SS} - 0.3$	—	0.8	V	TTL level
	V_{ILM}	MD0 to MD2	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
Open-drain output pin application voltage	V_D	PF6, PF7	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
“H” level output voltage	V_{OH}	D00 to D23 A00 to A31 P8 to PI (Except for PF6, PF7)	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$	4.0	—	—	V	
“L” level output voltage	V_{OL1}	D00 to D31 A00 to A23 P8 to PI (Except for PF6, PF7) (Except for PH4 to PH7) (Except for PI0 to PI2)	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 8.0\text{ mA}$	—	—	0.4	V	
	V_{OL2}	PH4 to PH7 PI0 to PI2	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 12.0\text{ mA}$	—	—	0.4	V	
	V_{OLD}	PF6, PF7	$V_{CC} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	D00 to D31 A00 to A23 P8 to PI	$V_{CC} = 5.5\text{ V}$ $0.45\text{ V} < V_I < V_{CC}$	—	—	± 5	μA	
Pull-up resistance	R_{PULL}	\overline{RST}	$V_{CC} = 5.5\text{ V}$ $V_I = 0.45\text{ V}$	25	50	100	$\text{k}\Omega$	
Power supply current	I_{CC}	V_{CC}	$F_C = 25\text{ MHz}$ $V_{CC} = 5.5\text{ V}$	—	—	180	mA	
	I_{CCS}		$F_C = 25\text{ MHz}$ $V_{CC} = 5.5\text{ V}$	—	—	100	mA	Sleep mode
Input capacitance	C_{IN}	Except for V_{CC} , V_{SS} , AV_{CC} , AV_{SS}	—	—	10	—	pF	

*1: Hysteresis input pins : \overline{HST} , \overline{NMI} , PE0 to PE4, PE6, PE7, PF1, PF2, PF4, PF5, PG1 to PG3, PH0 to PH3, \overline{RST}

*2: TTL level input pins :D00 to D31, RDY, BRQ, PAR0 to PAR3

MB91103 Series

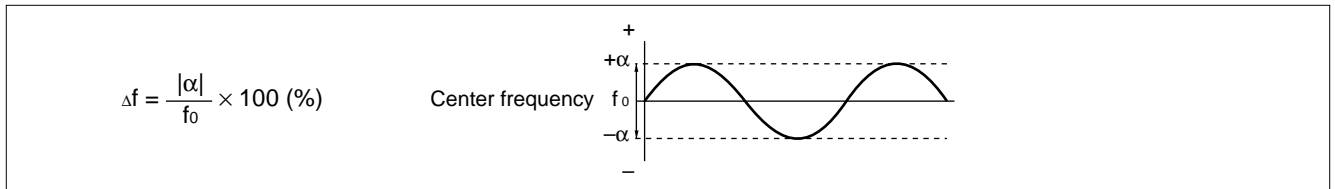
4. AC Characteristics

(1) Clock Timing Rating

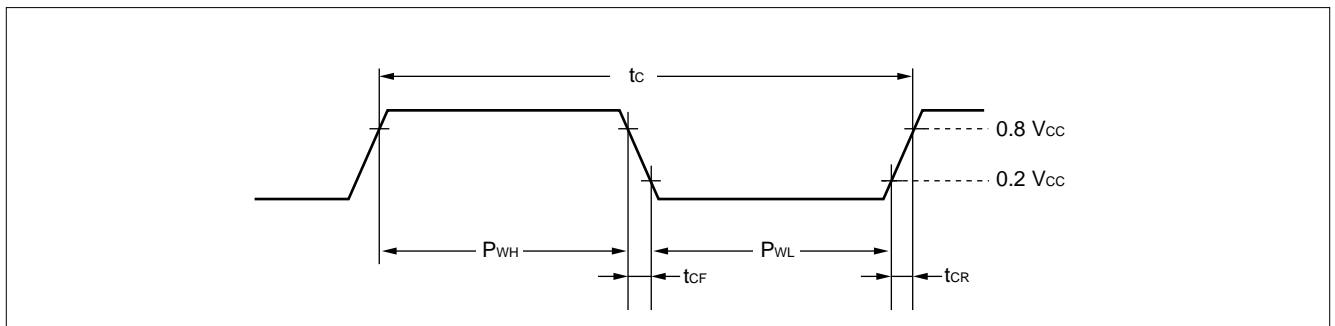
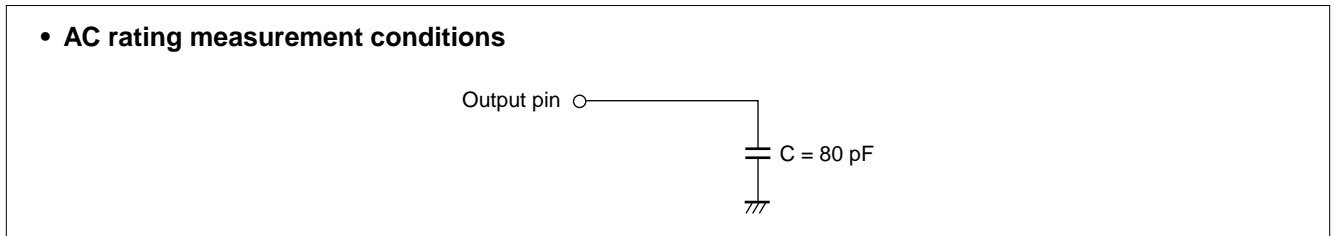
(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = -10°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F _C	X0 X1	—	10	50	MHz	
Clock cycle time	t _c	X0 X1		20	100	ns	
Frequency shift ratio (when locked) *1	Δf	—		—	5	%	
Input clock pulse width	P _{WH} P _{WL}	X0		8.5	—	ns	
Input clock rising/falling time	t _{CR} t _{CF}	X0		—	8	ns	t _{CR} + t _{CF}
Internal operating clock frequency	f _{CP}	—		0.625 *2	25	MHz	CPU system
	f _{CPP}	—		0.625 *2	25	MHz	Peripheral system
Internal operating clock cycle time	t _{CP}	—		40	1600 *2	ns	CPU system
	t _{CPP}	—		40	1600 *2	ns	Peripheral system

*1: Frequency shift ratio stands for deviation ratio of the operating clock from the center frequency in the clock multiplication system.



*2: These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.



MB91103 Series

(2) Clock Output Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
CLK $\uparrow \rightarrow$ CLK \downarrow	t_{CHCL}	CLK		$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*2
CLK $\downarrow \rightarrow$ CLK \uparrow	t_{CLCH}	CLK		$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*3

*1: t_{CYC} is a frequency for 1 clock cycle including a gear cycle.

*2: This rating is for a gear cycle of $\times 1$.

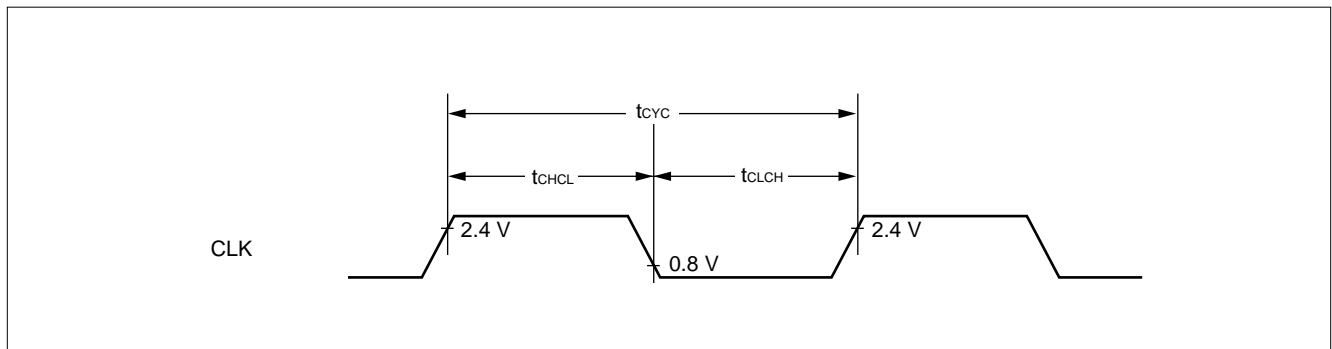
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute n of the following equations with 1/2, 1/4, 1/8, respectively.

- Min. : $(1 - n/2) \times t_{CYC} - 10$
- Max. : $(1 - n/2) \times t_{CYC} + 10$

*3: This rating is for a gear cycle of $\times 1$.

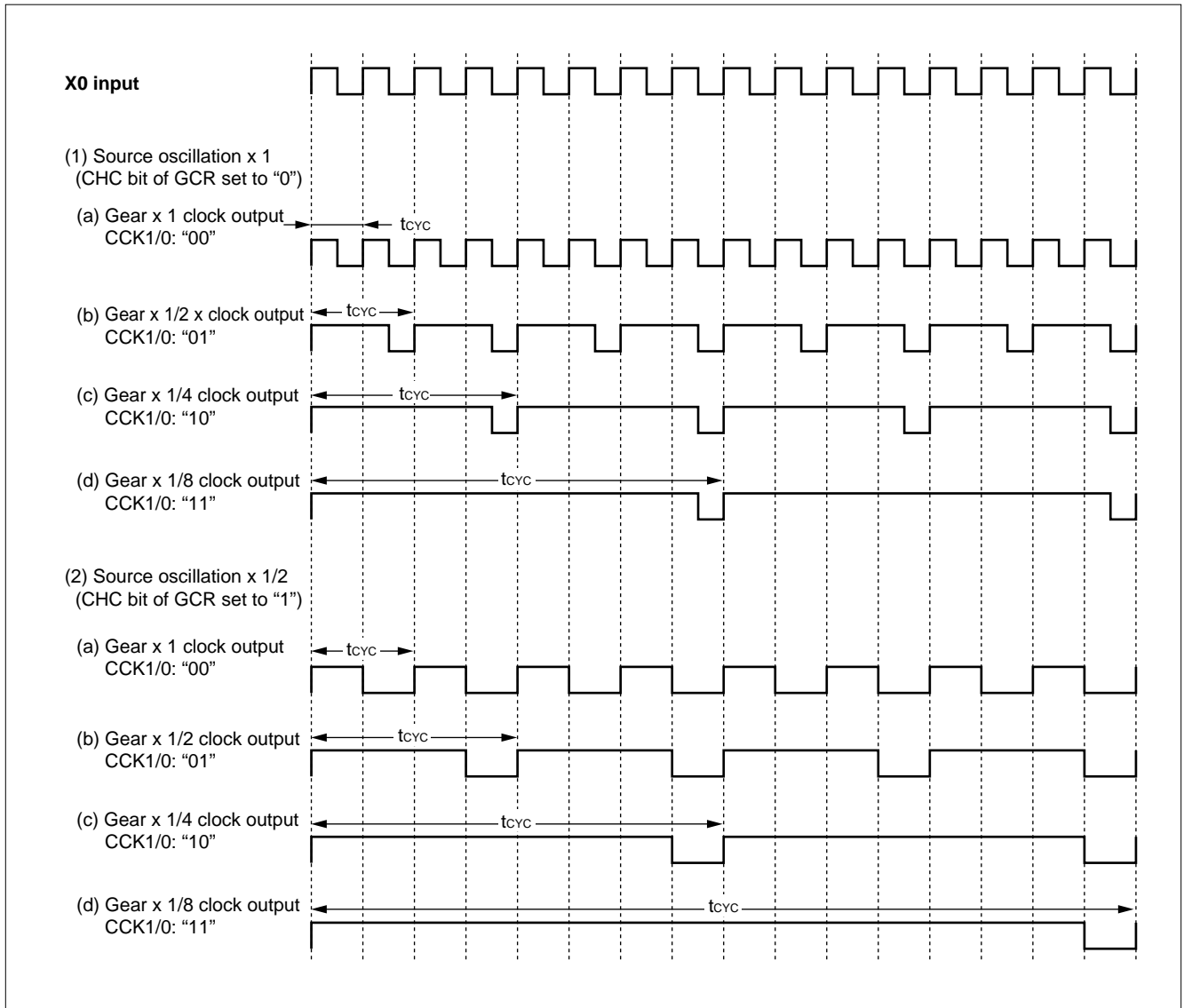
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute n of the following equations with 1/2, 1/4, 1/8, respectively.

- Min. : $n/2 \times t_{CYC} - 10$
- Max. : $n/2 \times t_{CYC} + 10$



MB91103 Series

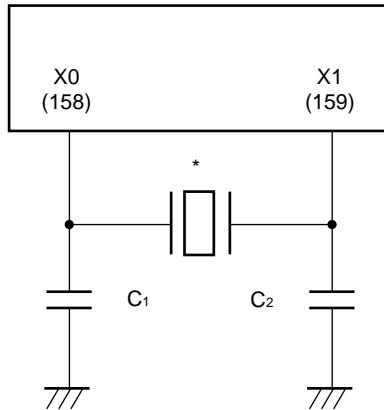
The relation between X0 input and clock output for configured by CHC/CCK1/CCK0 settings of GCR (Gear control register) is as follows:



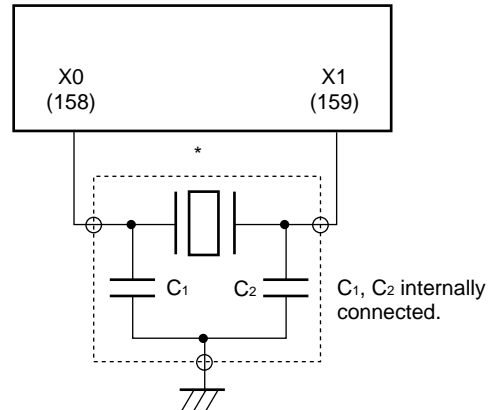
MB91103 Series

• **Ceramic oscillator applications**

Recommended circuit (2 contacts)



Recommended circuit (3 contacts)



* : Murata Mfg. Co., Ltd.

• **Discreet type**

Frequency range [MHz]	Model	Circuit parameter				Contact type
		C1 [pF]	C2 [pF]	Rf *1 [Ω]	Rd *2 [Ω]	
10.00 to 13.00	CSA □ MTZ	30	30	—	0	2 contacts
	CST □ MTW	(30)	(30)	—	0	3 contacts
13.01 to 15.99	CSA □ MXZ040	15	15	—	0	2 contacts
	CST □ MXW0C3	(15)	(15)	—	0	3 contacts
16.00 to 19.99	CSA □ MXZ040	10	10	—	0	2 contacts
	*****	*****	*****	*****	*****	3 contacts
20.00 to 25.00	CSA □ MXZ040	5	5	—	0	2 contacts
	CST □ MXW0H1	(5)	(5)	—	0	3 contacts

*1: Feed-back resistance Rf internally connected in LSI.

*2: No damping resistance required.

(): C1 and C2 internally connected.

MB91103 Series

- SMD type

Frequency range [MHz]	Model	Circuit parameter				Contact type
		C1 [pF]	C2 [pF]	Rf *1 [Ω]	Rd *2 [Ω]	
10.00 to 13.00	CSACS □ MT	30	30	—	0	2 contacts
	CSTCS □ MT	(30)	(30)	—	0	3 contacts
13.01 to 15.99	CSACS □ MX040	15	15	—	0	2 contacts
	CSTCS □ MX0C3	(15)	(15)	—	0	3 contacts
16.00 to 19.99	CSACS □ MX040	10	10	—	0	2 contacts
	CSTCS □ MX0C2	(10)	(10)	—	0	3 contacts
20.00 to 25.00	CSACS □ MX040	5	5	—	0	2 contacts
	CSTCS □ MX0H1	(5)	(5)	—	0	3 contacts

*1: Feed-back resistance Rf internally connected in LSI.

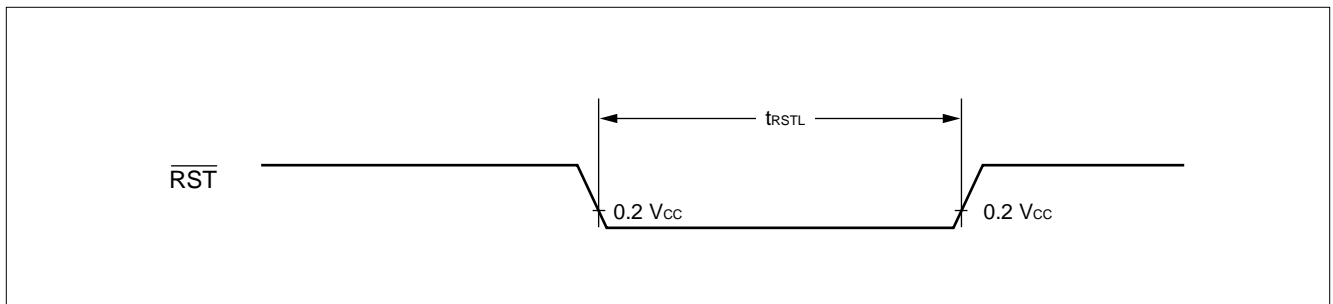
*2: No damping resistance required.

(): C₁ and C₂ internally connected.

(3) Reset Input

(V_{CC} = +5.0 V ±10%, V_{SS} = 0.0 V, T_A = -10°C to +70°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t _{RSTL}	$\overline{\text{RST}}$	—	t _{CP} × 5	—	ns	

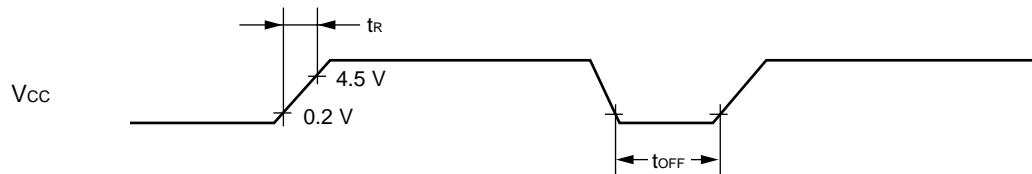


MB91103 Series

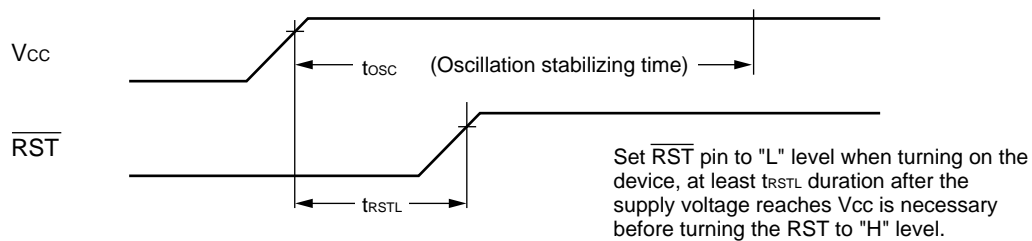
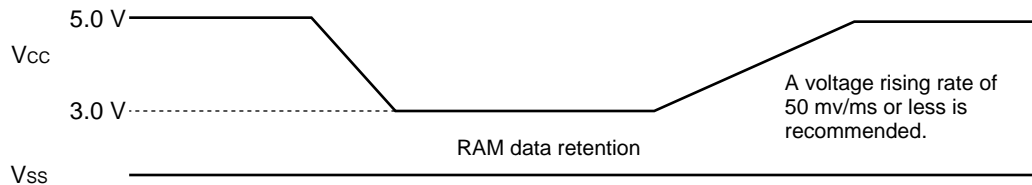
(4) Power-on Reset

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	—	30	ms	$V_{CC} < 0.2\text{ V}$ before turning power supply
Power supply shut off time	t_{OFF}	V_{CC}		1	—	ms	For repeated operations
Oscillation stabilizing time	t_{OSC}	—		$2 \times t_c \times 2^{21}$	—	ns	



Sudden change in supply voltage during operation may initiate a power-on sequence.
To change supply voltage during operation, it is recommended to smoothly raise the voltage
to avoid rapid fluctuations in the supply voltage.



Set \overline{RST} pin to "L" level when turning on the device, at least t_{RSTL} duration after the supply voltage reaches V_{CC} is necessary before turning the RST to "H" level.

t_{RSTL} : Reset input time

MB91103 Series

(5) Normal Bus Access Read/write Operation

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{CS0}$ to $\overline{CS5}$ delay time	t_{CHCSL}	CLK	—	—	15	ns	
	t_{CHCSH}	$\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	t_{CHAV}	CLK A23 to A00		—	15	ns	
Data (parity) delay time	t_{CHDV}	CLK D31 to D00 PAR0 to PAR3		—	15	ns	
\overline{RD} delay time	t_{CLRL}	CLK		—	6	ns	
	t_{CLRH}	\overline{RD}		—	6	ns	
$\overline{WR0}$ to $\overline{WR3}$ delay time	t_{CLWL}	CLK		—	6	ns	
	t_{CLWH}	$\overline{WR0}$ to $\overline{WR3}$		—	6	ns	
Valid address → valid data (parity) input time	t_{AVDV}	A23 to A00 D31 to D00 PAR0 to PAR3		—	$\frac{3}{2} \times t_{CYC}$ – 25	ns	*1 *2
$\overline{RD} \downarrow \rightarrow$ valid data (parity) input time	t_{RLDV}			—	$t_{CYC} - 10$	ns	*1
Data (parity) set up → $\overline{RD} \uparrow$ time	t_{DSRH}	\overline{RD} D31 to D00 PAR0 to PAR3	10	—	ns		
$\overline{RD} \uparrow \rightarrow$ data (parity) hold time	t_{RHDX}		0	—	ns		

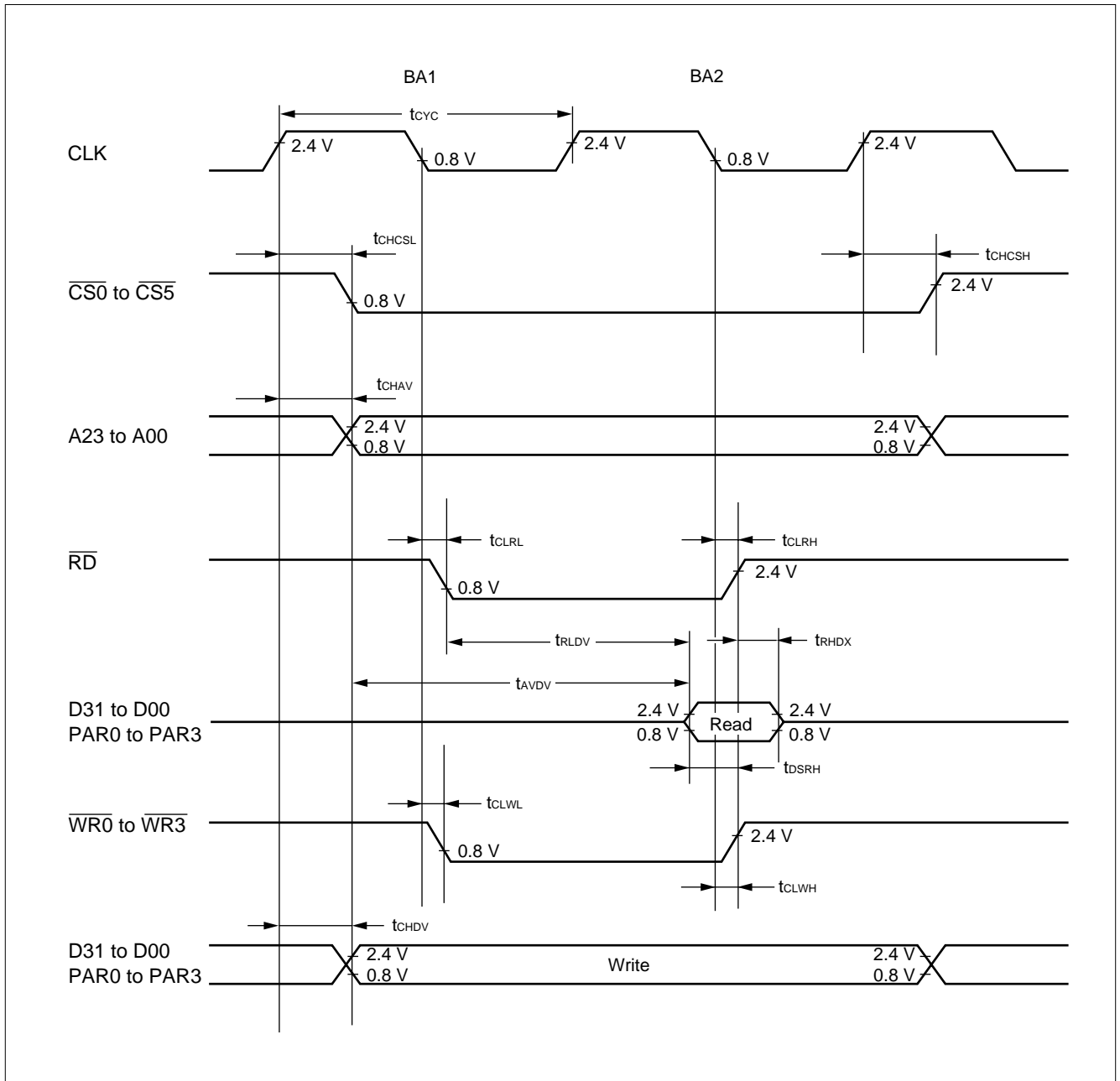
*1: When bus timing is delayed by automatic wait insertion or RDY input, add ($t_{CYC} \times$ extended cycle number for delay) to this rating.

*2: This rating is for a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute n in the following equation with 1/2, 1/4, 1/8, respectively.

- Equation: $(2 - n/2) \times t_{CYC} - 25$

MB91103 Series



MB91103 Series

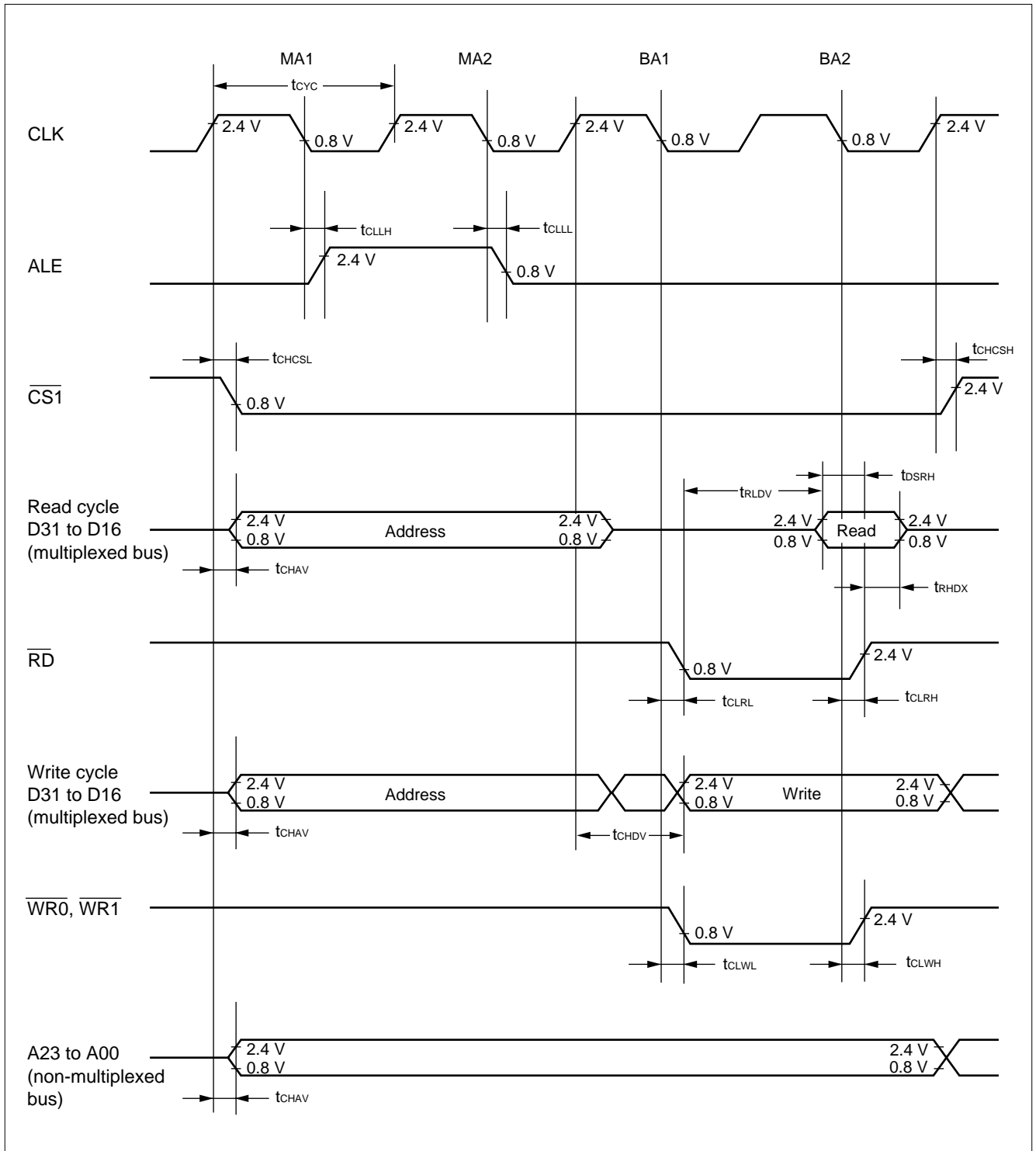
(6) Time-sharing Bus Read/Write Operation

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
ALE delay time	t _{CLLH}	CLK ALE	—	—	6	ns	
	t _{CLLL}	ALE		—	6	ns	
$\overline{\text{CS}}1$ delay time	t _{CHCSL}	CLK $\overline{\text{CS}}1$		—	15	ns	
	t _{CHCSH}	$\overline{\text{CS}}1$		—	15	ns	
Address delay time	t _{CHAV}	CLK D31 to D16		—	15	ns	
Data delay time	t _{CHDV}	CLK D31 to D16		—	15	ns	
$\overline{\text{RD}}$ delay time	t _{CLRL}	CLK $\overline{\text{RD}}$		—	6	ns	
	t _{CLRH}	$\overline{\text{RD}}$		—	6	ns	
$\overline{\text{WR}}0, \overline{\text{WR}}1$ delay time	t _{CLWL}	CLK $\overline{\text{WR}}0, \overline{\text{WR}}1$		—	6	ns	
	t _{CLWH}	$\overline{\text{WR}}0, \overline{\text{WR}}1$		—	6	ns	
$\overline{\text{RD}} \downarrow \rightarrow$ valid data input time	t _{RLDV}	$\overline{\text{RD}}$		—	t _{CYC} - 10	ns	*
Data set up $\rightarrow \overline{\text{RD}} \uparrow$ time	t _{DSRH}	$\overline{\text{RD}}$ D31 to D16		10	—	ns	
$\overline{\text{RD}} \uparrow \rightarrow$ data hold time	t _{RHDX}		0	—	ns		

* : When bus timing is delayed by automatic wait insertion or RDY input, add (t_{CYC} × extended cycle number for delay) to this rating.

MB91103 Series

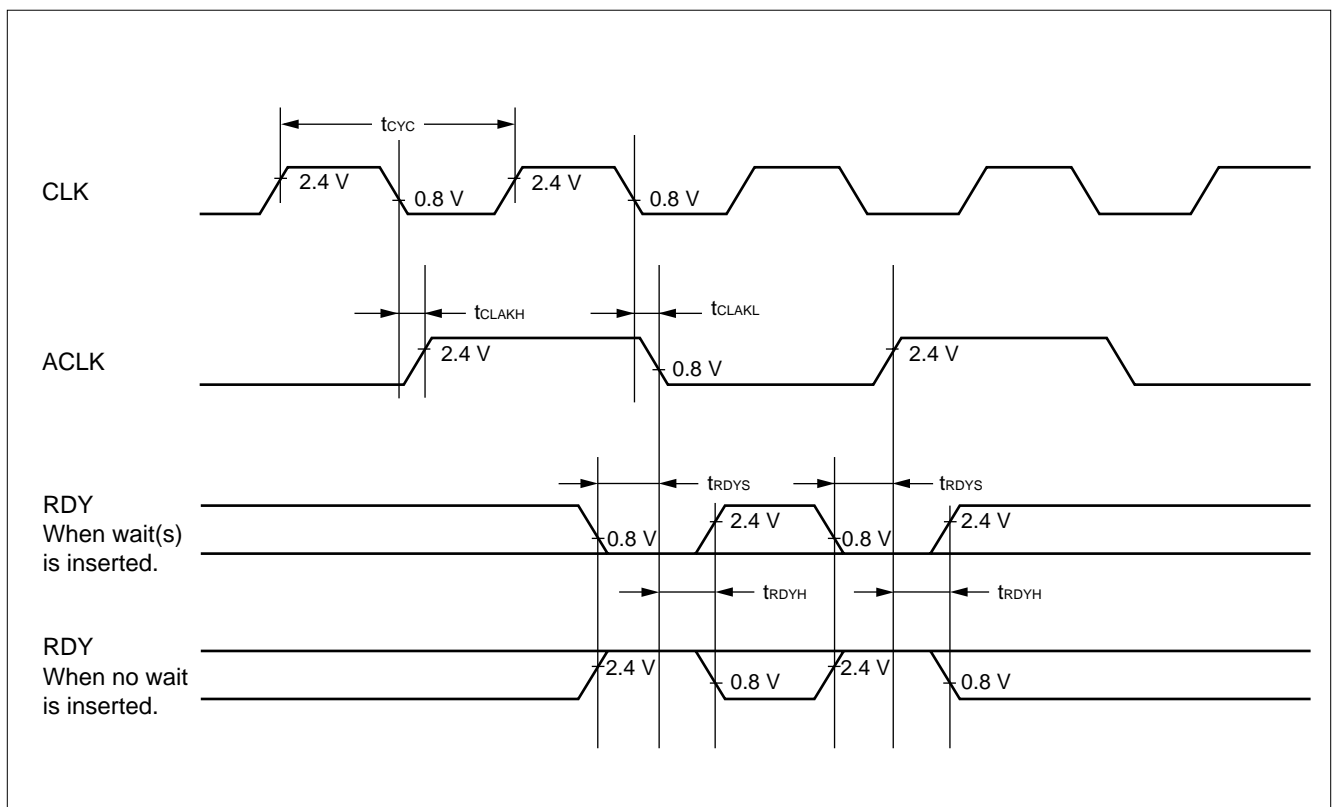


MB91103 Series

(7) Ready Input Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
ACLK delay time	t_{CLAKH}	CLK ACLK	—	—	6	ns	
	t_{CLAKL}	ACLK		—	6	ns	
RDY set up time \rightarrow ACLK $\uparrow\downarrow$	t_{RDYS}	RDY ACLK		10	—	ns	
ACLK $\uparrow\downarrow \rightarrow$ RDY hold time	t_{RDYH}	ACLK RDY		0	—	ns	



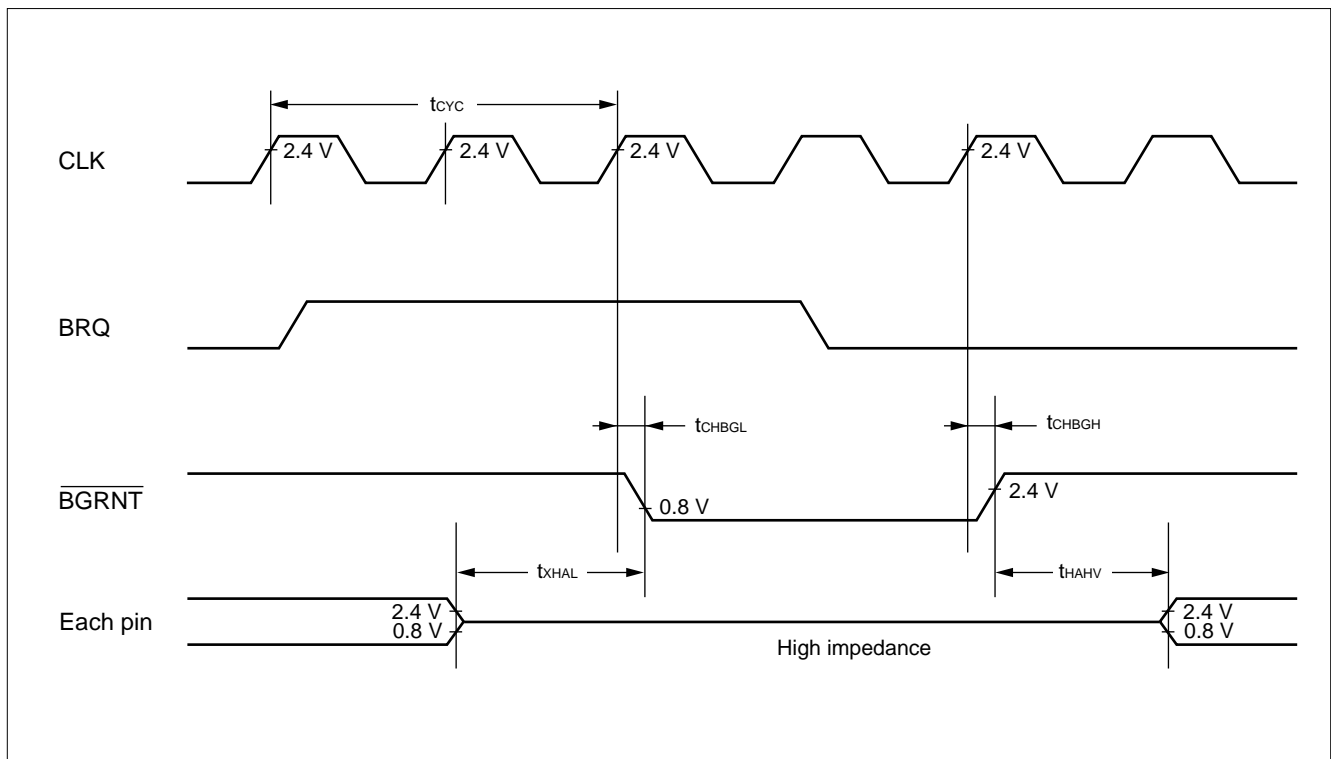
MB91103 Series

(8) Hold Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	CLK	—	—	6	ns	
	t_{CHBGH}	$\overline{\text{BGRNT}}$		—	6	ns	
Pin floating \rightarrow $\overline{\text{BGRNT}}$ \downarrow time	t_{XHAL}	$\overline{\text{BGRNT}}$	—	$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	
$\overline{\text{BGRNT}}$ \uparrow \rightarrow pin valid time	t_{HAHV}			$t_{\text{CYC}} - 10$	$t_{\text{CYC}} + 10$	ns	

Note: There is a delay time of more than 1 cycle from BRQ input to $\overline{\text{BGRNT}}$ change.



MB91103 Series

(9) Normal DRAM Mode Read/Write Cycle

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	6	ns	
	t_{CHRAL}			—	6	ns	
CAS delay time	t_{CLCASL}	CLK CAS		—	6	ns	
	t_{CLCASH}			—	6	ns	
ROW address delay time	t_{CHRAV}	CLK A23 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV}			—	15	ns	
\overline{DW} delay time	t_{CHDWL}	CLK \overline{DW}		—	15	ns	
	t_{CHDWH}			—	15	ns	
Output data (parity) delay time	t_{CHDV1}	CLK D31 to D00 PAR0 to PAR3		—	15	ns	
RAS $\downarrow \rightarrow$ valid data (parity) input time	t_{RLDV}	RAS D31 to D00 PAR0 to PAR3		—	$5/2 \times t_{CYC}$ – 16	ns	*1 *2
CAS $\downarrow \rightarrow$ valid data (parity) input time	t_{CLDV}	CAS D31 to D00 PAR0 to PAR3		—	$t_{CYC} - 10$	ns	*1
CAS $\uparrow \rightarrow$ data (parity) hold time	t_{CADH}			0	—	ns	

CAS: CS0L to CS1H pins are for CAS signal outputs.

\overline{DW} : $\overline{DW0}$, $\overline{DW1}$ and CS0H to CS1H are used for \overline{WE} outputs.

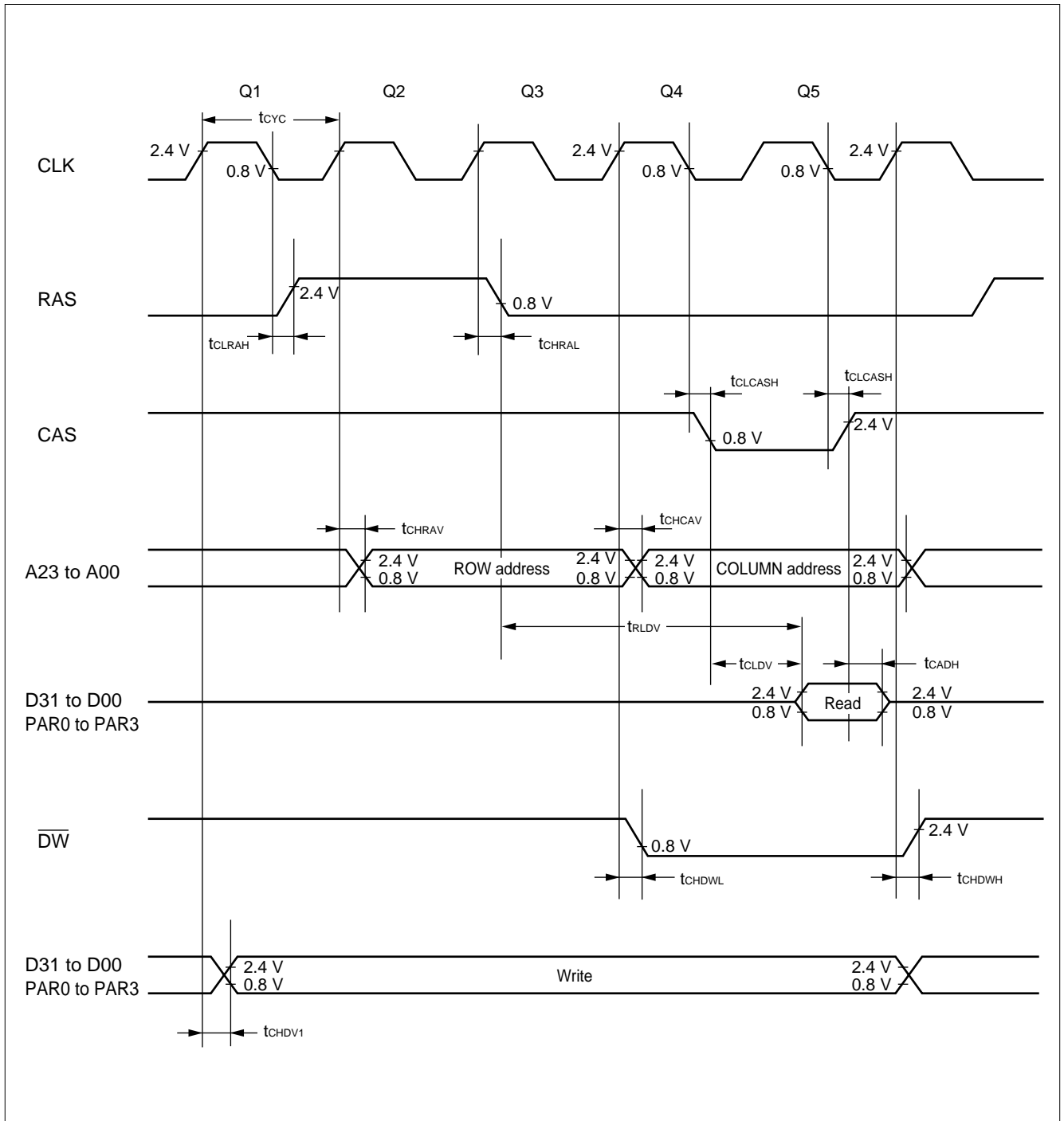
*1: When Q1 cycle or Q4 cycle is extended for “1” cycle, add t_{CYC} time to this rating.

*2: This rating is for a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

- Equation: $(3 - n/2) \times t_{CYC} - 16$

MB91103 Series



MB91103 Series

(10) Normal DRAM Mode Fast Page Read/Write Cycle

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

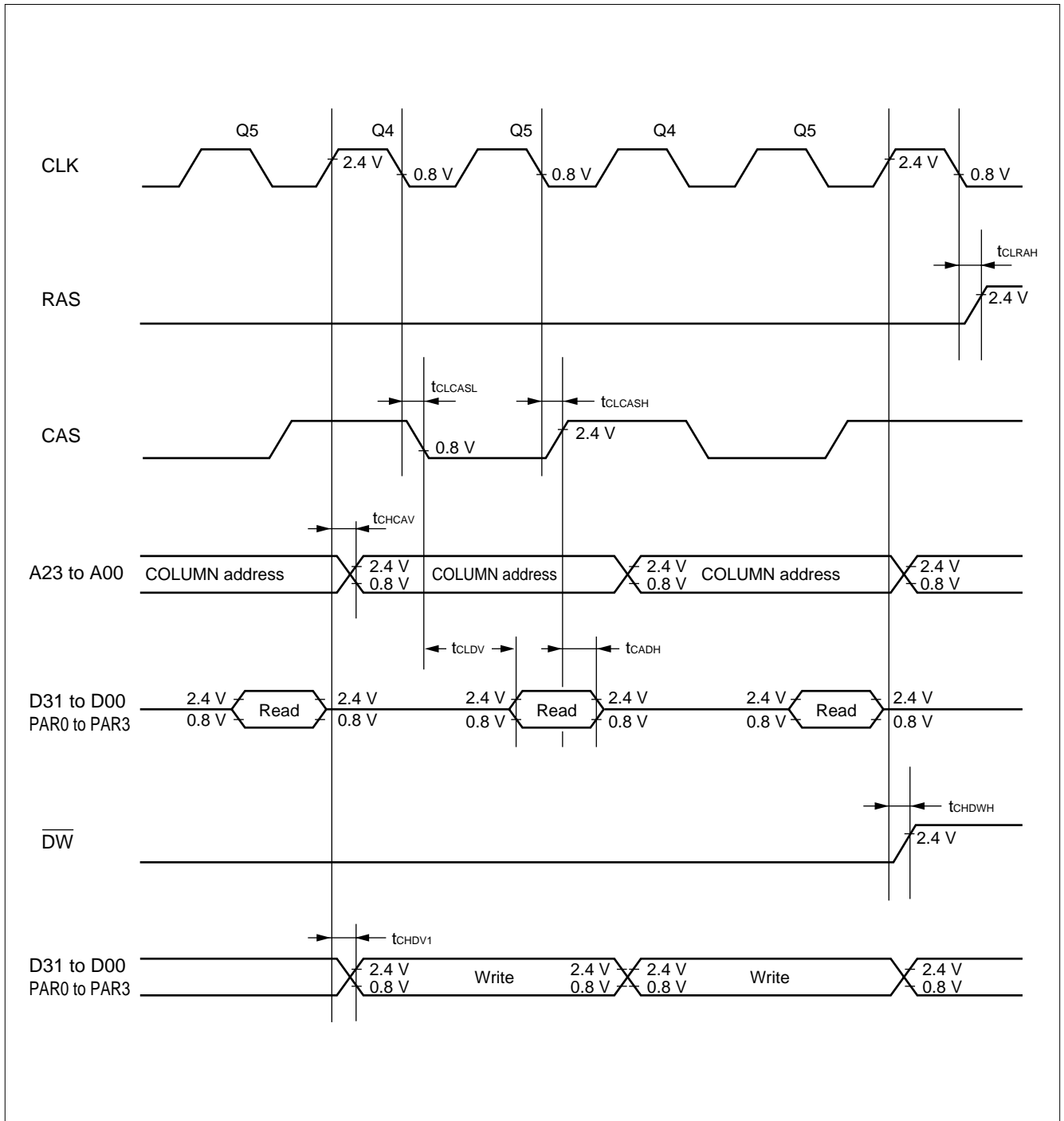
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	6	ns	
CAS delay time	t_{CLCASL}	CLK		—	6	ns	
	t_{CLCASH}	CAS		—	6	ns	
COLUMN address delay time	t_{CHCAV}	CLK A23 to A00		—	15	ns	
\overline{DW} delay time	t_{CHDWH}	CLK \overline{DW}		—	15	ns	
Output data (parity) delay time	t_{CHDV1}	CLK D31 to D00 PAR0 to PAR3		—	15	ns	
CAS $\downarrow \rightarrow$ valid data (parity) input time	t_{CLDV}	CAS D31 to D00 PAR0 to PAR3		—	$t_{CYC} - 10$	ns	*
CAS $\uparrow \rightarrow$ data (parity) hold time	t_{CADH}		0	—	ns		

CAS: CS0L to CS1H pins are for CAS signal outputs.

\overline{DW} : $\overline{DW0}$, $\overline{DW1}$ and CS0H to CS1H are used for \overline{WE} outputs.

* : When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

MB91103 Series



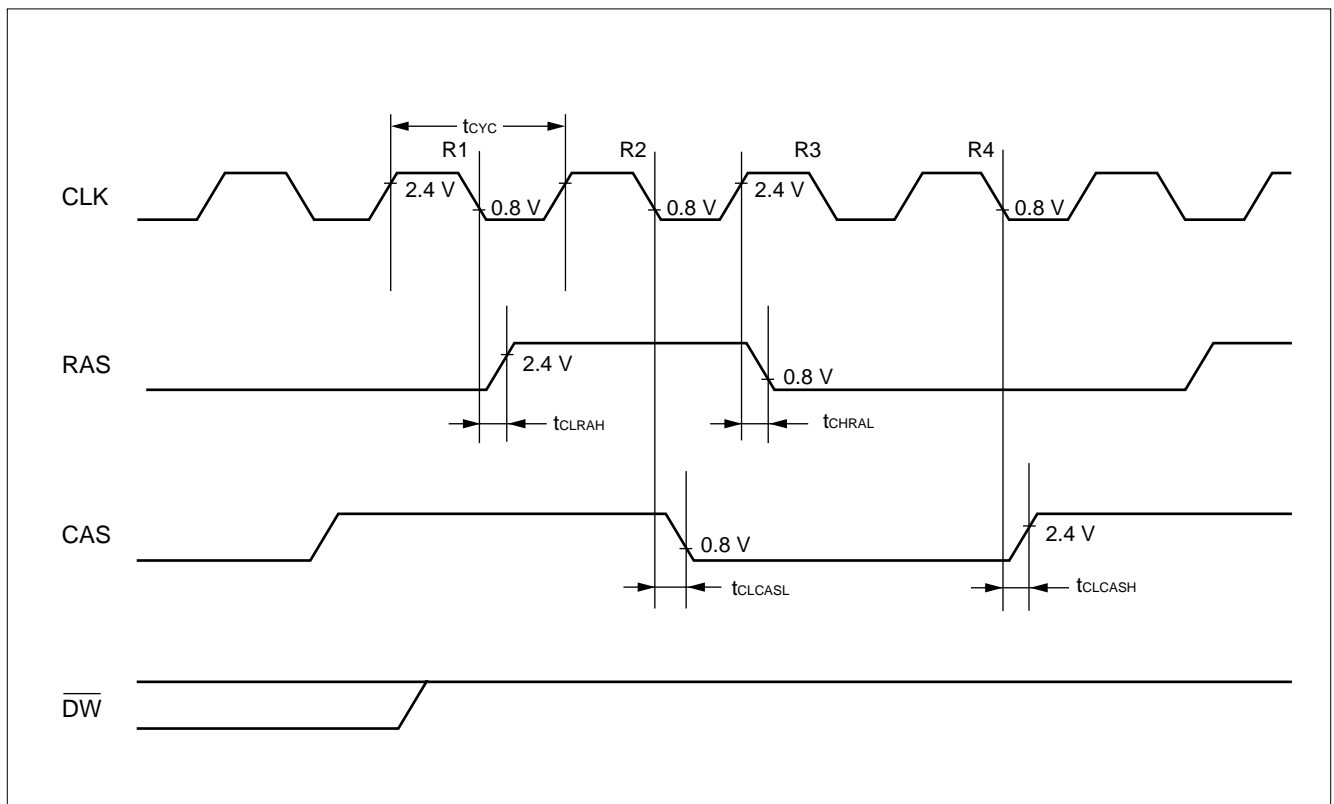
MB91103 Series

(11) CBR Refresh

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	6	ns	
	t_{CHRAL}			—	6	ns	
CAS delay time	t_{CLCASL}	CLK CAS	—	—	6	ns	
	t_{CLCASH}			—	6	ns	

CAS: CS0L to CS1H pins are for CAS signal outputs.



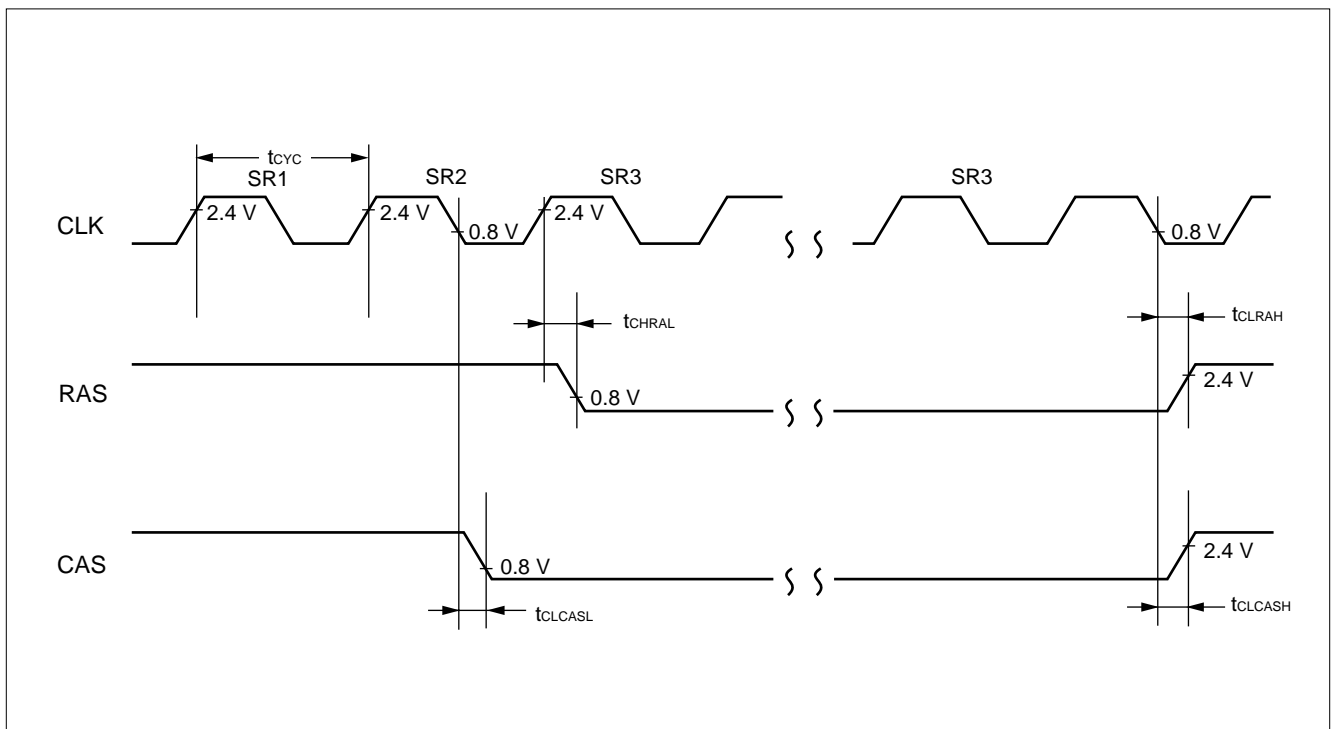
MB91103 Series

(12) Self Refresh

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	6	ns	
	t_{CHRAL}			—	6	ns	
CAS delay time	t_{CLCASL}	CLK CAS	—	—	6	ns	
	t_{CLCASH}			—	6	ns	

CAS: CS0L to CS1H pins are for CAS signal outputs.



MB91103 Series

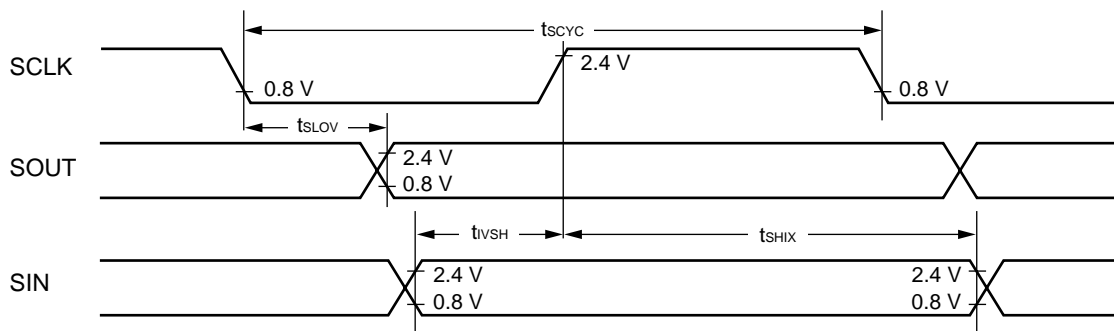
(13) UART Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

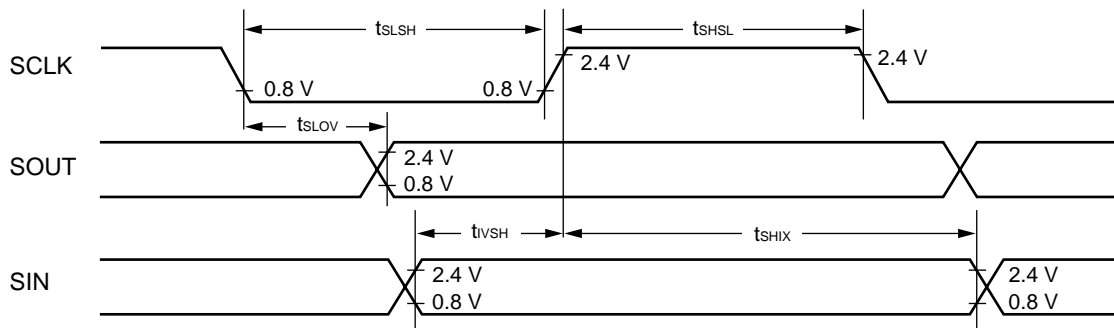
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	$8 t_{CYCP}$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	—		-80	80	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{VSH}	—		100	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode	$4 t_{CYCP}$	—	ns	
Serial clock "L" pulse width	t_{LSLH}	—		$4 t_{CYCP}$	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{VSH}	—		60	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	—		60	—	ns	

- Notes:
- This rating is for AC characteristics in CLK synchronous mode.
 - t_{CYCP} is a cycle time of peripheral system clock.

• Internal shift clock mode



• External shift clock mode



MB91103 Series

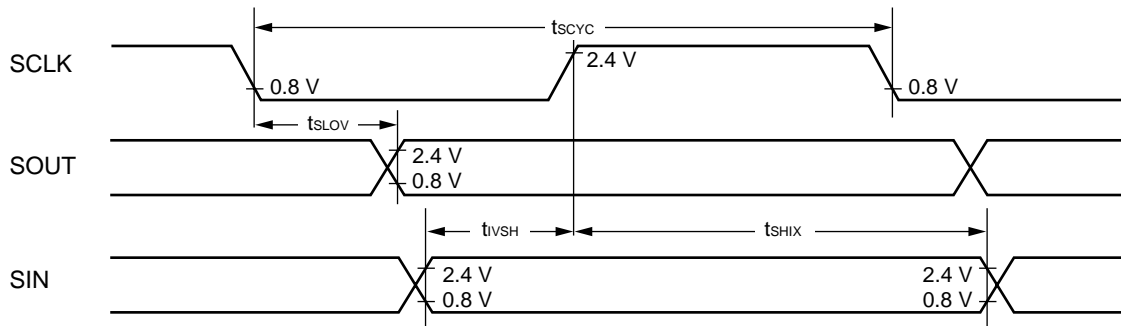
(14) I/O Extended Serial Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

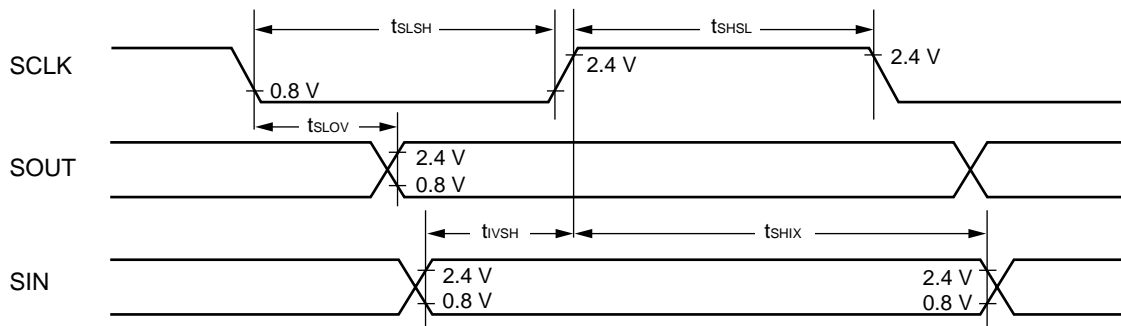
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	$8 t_{CYCP}$	—	ns	Max. external frequency is 2 MHz
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	—		—	80	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{VSH}	—		$1 t_{CYCP}$	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	—		$1 t_{CYCP}$	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode	230	—	ns	
Serial clock "L" pulse width	t_{SLSH}	—		230	—	ns	
SCLK $\downarrow \rightarrow$ SOUT delay time	t_{SLOV}	—		—	$2 t_{CYCP}$	ns	
Valid SIN \rightarrow SCLK \uparrow	t_{VSH}	—		$1 t_{CYCP}$	—	ns	
SCLK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	—		$2 t_{CYCP}$	—	ns	

Note: t_{CYCP} is a cycle time of peripheral system clock.

• Internal shift clock mode



• External shift clock mode



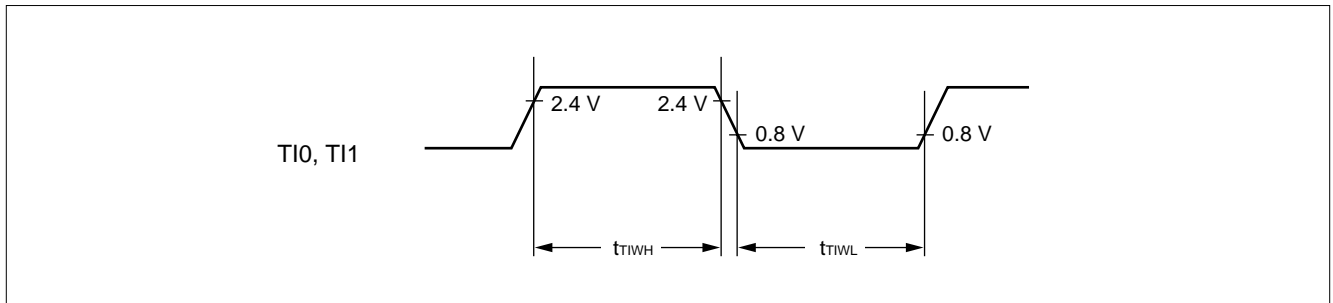
MB91103 Series

(15) Timer System Input Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	TI0, TI1	—	$2 t_{CYCP}$	—	ns	

Note: t_{CYCP} is a cycle time of peripheral system clock.

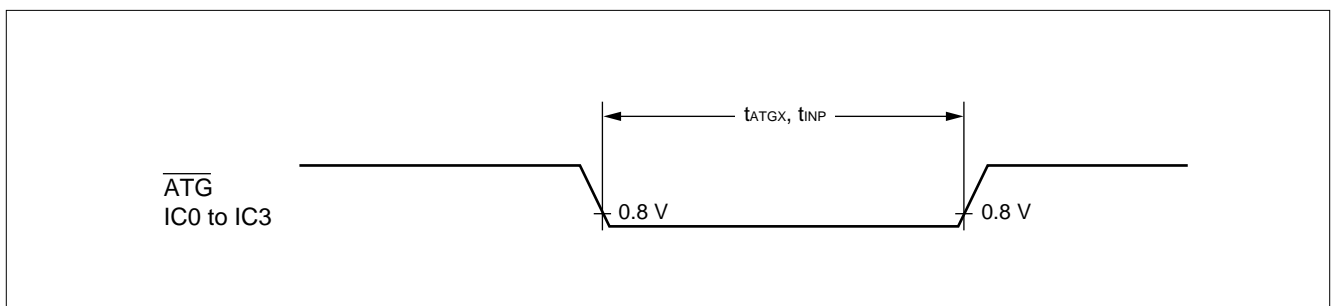


(16) Trigger System Input Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
A/D start trigger input time	t_{ATGX}	\overline{ATG}	—	$5 t_{CYCP}$	—	ns	
Input capture input trigger	t_{INP}	IC0 to IC3		$5 t_{CYCP}$	—	ns	

Note: t_{CYCP} is a cycle time of peripheral system clock.



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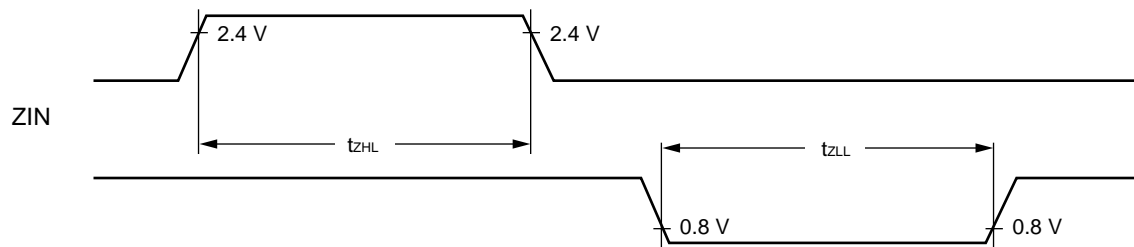
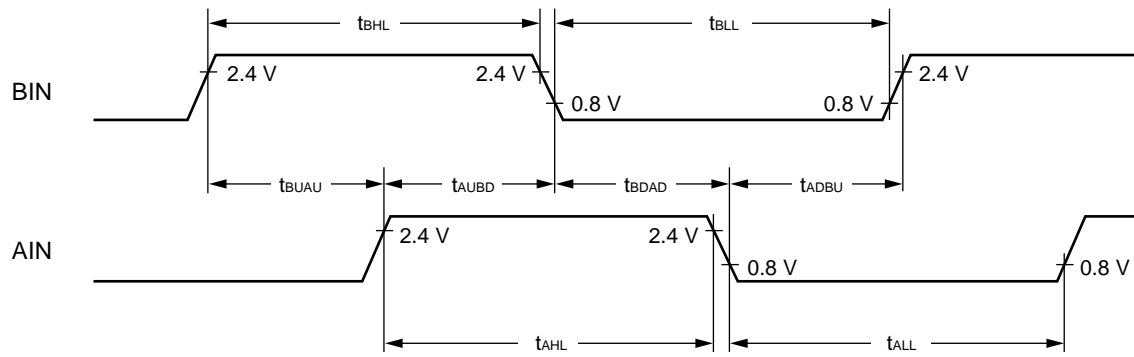
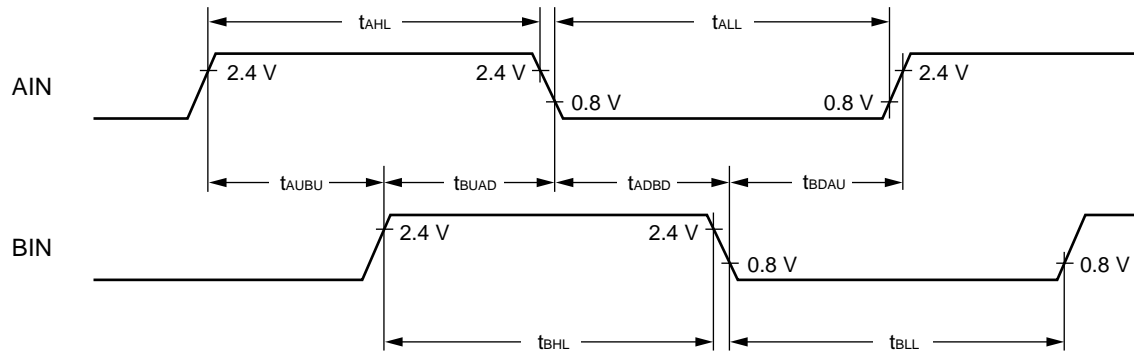
(17) Up/Down Counter Input Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
AIN input "1" pulse width	t _{AHL}	AIN0 AIN1 BIN0 BIN1	—	8 t _{CYCP}	—	ns	
AIN input "0" pulse width	t _{ALL}			8 t _{CYCP}	—	ns	
BIN input "1" pulse width	t _{BHL}			8 t _{CYCP}	—	ns	
BIN input "0" pulse width	t _{BLL}			8 t _{CYCP}	—	ns	
AIN \uparrow → BIN \uparrow time	t _{AUBU}			4 t _{CYCP}	—	ns	
BIN \uparrow → AIN \downarrow time	t _{BUAD}			4 t _{CYCP}	—	ns	
AIN \downarrow → BIN \downarrow time	t _{ADBD}			4 t _{CYCP}	—	ns	
BIN \downarrow → AIN \uparrow time	t _{BDAU}			4 t _{CYCP}	—	ns	
BIN \uparrow → AIN \uparrow time	t _{BUAU}			4 t _{CYCP}	—	ns	
AIN \uparrow → BIN \downarrow time	t _{AUBD}			4 t _{CYCP}	—	ns	
BIN \downarrow → AIN \downarrow time	t _{BDAD}			4 t _{CYCP}	—	ns	
AIN \downarrow → BIN \uparrow time	t _{ADBU}			4 t _{CYCP}	—	ns	
ZIN input "1" pulse width	t _{ZHL}	ZIN0		4 t _{CYCP}	—	ns	
ZIN input "0" pulse width	t _{ZLL}	ZIN1		4 t _{CYCP}	—	ns	

Note: t_{CYCP} is a cycle time of peripheral system clock.

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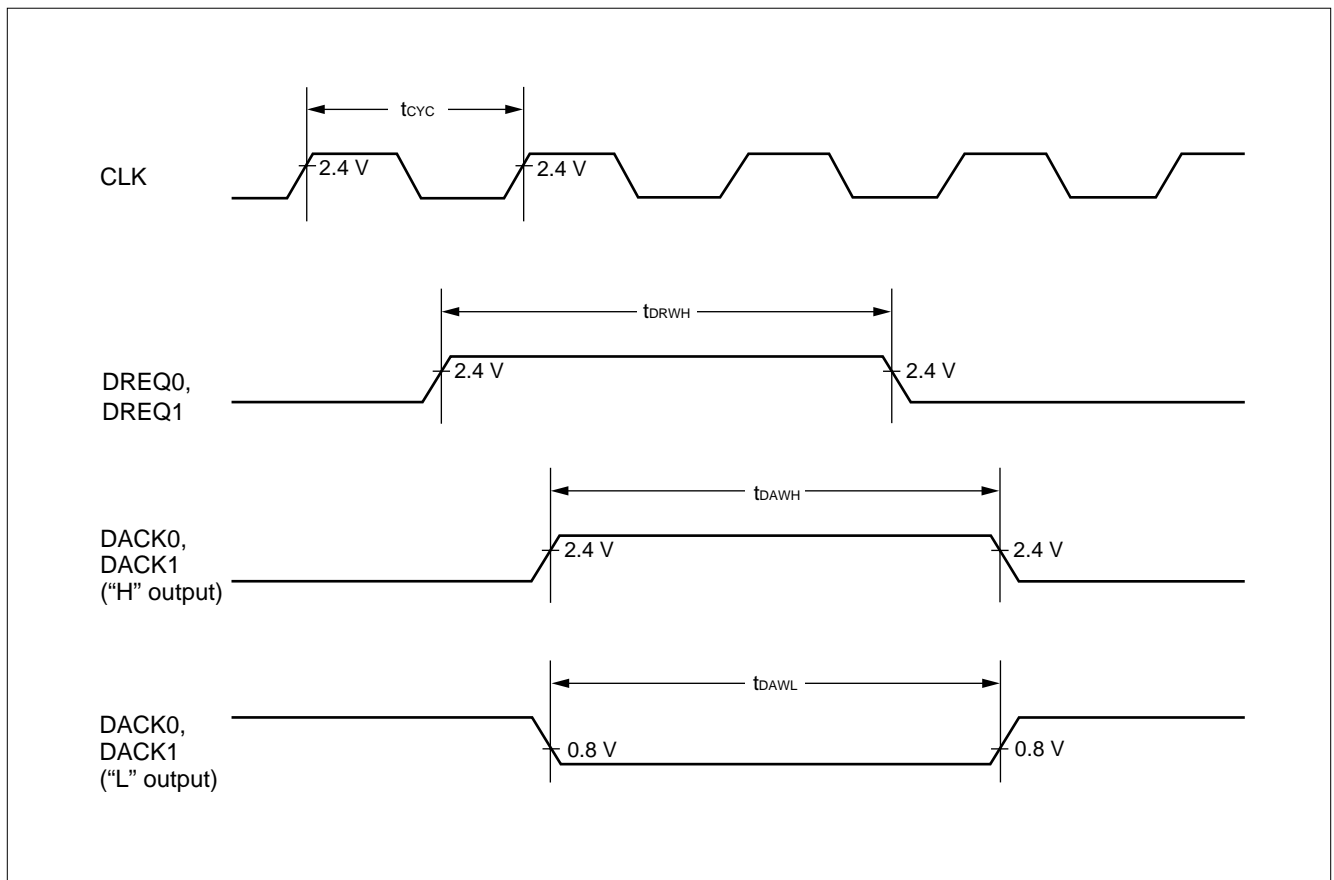


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(18) DMA Controller Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
DREQ input pulse width	t_{DRWH}	DREQ0 DREQ1	—	$2 t_{CYC}$	—	ns	
DACK "H" output pulse width	t_{DAWH}	DACK0 DACK1		t_{CYC}	$3 t_{CYC}$	ns	
DACK "L" output pulse width	t_{DAWL}	DACK0 DACK1		t_{CYC}	$3 t_{CYC}$	ns	



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5. A/D Conversion Block Electrical Characteristics

($AV_{CC} = V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -10^\circ\text{C to }+70^\circ\text{C}$, $+4.5\text{ V} \leq AV_{RH} - AV_{RL}$)

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	BIT
Total error	—	—	—	—	± 3.0	LSB
Linearity error	—	—	—	—	± 2.0	LSB
Differentiation linearity error	—	—	—	—	± 1.5	LSB
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{RL} - 1.5$	$AV_{RL} + 0.5$	$AV_{RL} + 2.5$	LSB
Full-scale transition voltage	V_{FST}	AN0 to AN7	$AV_{RH} - 4.5$	$AV_{RH} - 1.5$	$AV_{RH} + 0.5$	LSB
Conversion time	—	—	5.6 *1	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	μA
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{RL}	—	AV_{RH}	V
		Reference voltage	—	AV_{RH}	AV_{RL}	—
Reference voltage	—	AVRH	AV_{RL}	—	AV_{CC}	V
		AVRL	AV_{SS}	—	AV_{RH}	V
Power supply current	I_A	AV_{CC}	—	4	—	mA
			I_{AH}	—	—	5 *2
Reference voltage supply current	I_R	AVRH	—	200	—	μA
			I_{RH}	—	—	170 *2
Conversion variance between channels	—	AN0 to AN7	—	—	4	LSB

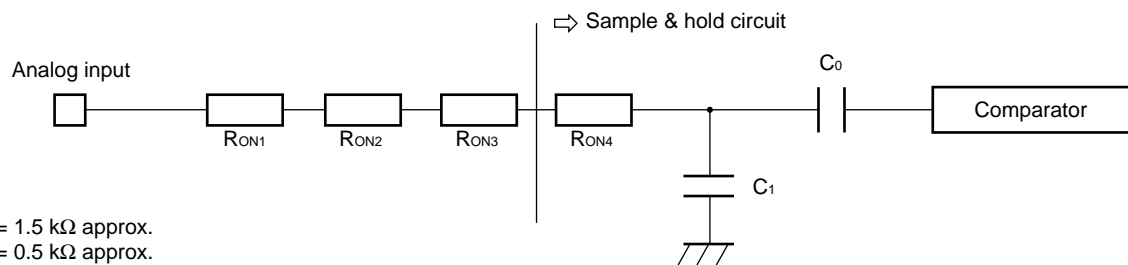
*1: $V_{CC} = 5.0\text{ V} \pm 10\%$, machine clock of 25 MHz

*2: Current value for A/D converters not in operation, CPU stop mode ($V_{CC} = AV_{CC} = AV_{RH} = 5.0\text{ V}$)

- Notes:
- As the absolute value of $|AV_{RH}-AV_{RL}|$ decreases, relative error increases.
 - Output impedance of external circuit of analog input under following conditions;
Output impedance of external circuit < 7 k Ω approx.

If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling (sampling time is 5.6 μs for a machine clock of 25 MHz).

• Analog input circuit model plan

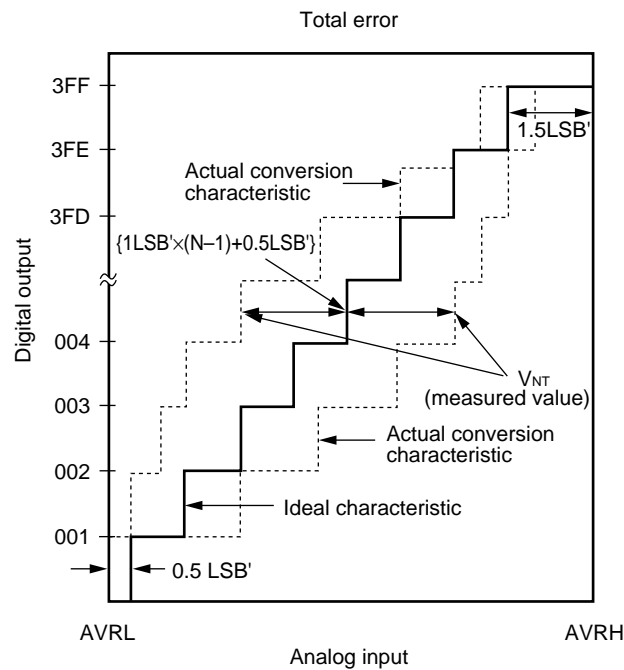


$R_{ON1} = 1.5\text{ k}\Omega$ approx.
 $R_{ON2} = 0.5\text{ k}\Omega$ approx.
 $R_{ON3} = 0.5\text{ k}\Omega$ approx.
 $R_{ON4} = 0.5\text{ k}\Omega$ approx.
 $C_0 = 60\text{ pF}$ approx.
 $C_1 = 4\text{ pF}$ approx.

Note: Listed values are for reference purposes only.

6. Definitions of A/D Converter Descriptions

- Resolution
The smallest change in analog voltage detected by A/D converter.
- Linearity error
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 00001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”).
- Differential linearity error
A deviation of a step voltage for changing the LSB of output code from ideal input voltage.
- Total error
A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$1\text{LSB}' \text{ (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1 \text{LSB}' \times (N - 1) + 0.5 \text{LSB}'\}}{1 \text{LSB}'}$$

$$V_{0T}' \text{ (Ideal value)} = \text{AVRL} + 0.5 \text{LSB}' \text{ [V]}$$

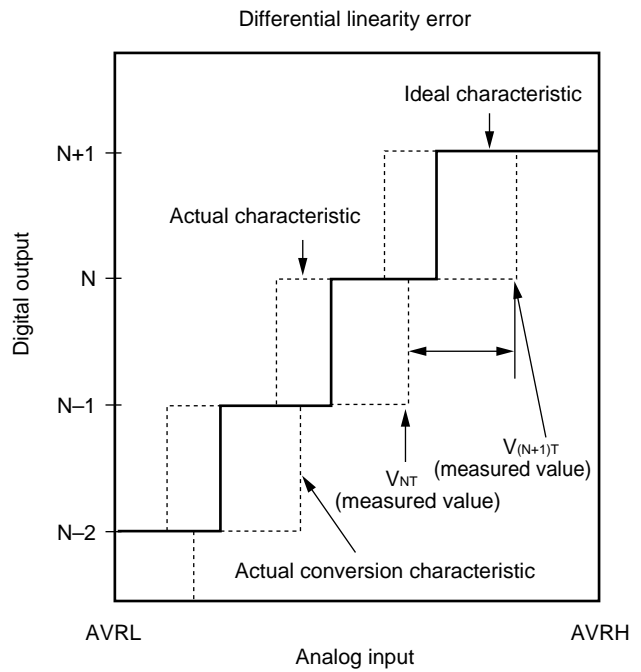
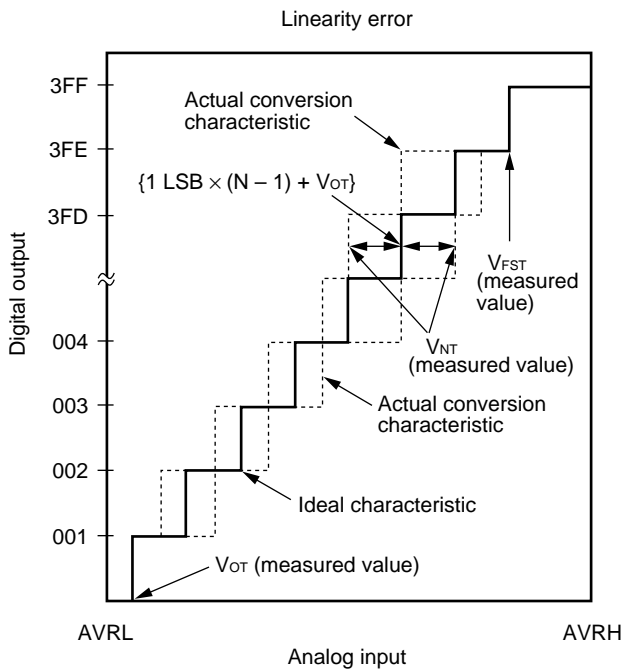
$$V_{FST}' \text{ (Ideal value)} = \text{AVRL} + 1.5 \text{LSB}' \text{ [V]}$$

V_{NT} : A voltage for causing transition of digital output from (N-1) to N

(Continued)

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(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}}$$

[LSB]

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

[LSB]

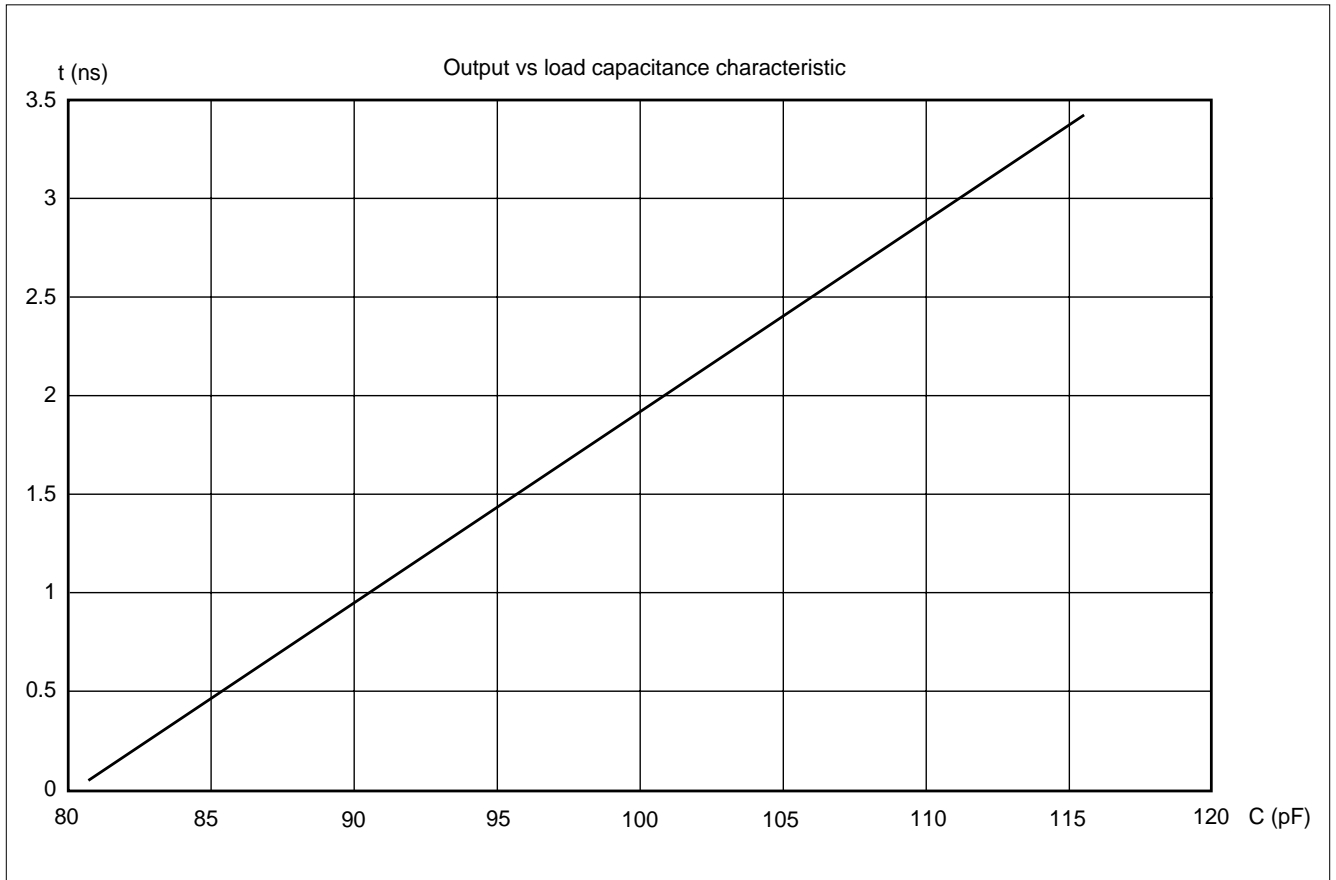
$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

V_{OT} : A voltage for causing transition of digital output from (000)_H to (001)_H

V_{FST} : A voltage for causing transition of digital output from (3FE)_H to (3FF)_H

MB91103 Series

■ OUTPUT VS LOAD CAPACITANCE CHARACTERISTIC



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■ INSTRUCTIONS

1. How to Read Instruction Set Summary

Mnemonic	Type	OP	~	NZVC	Operation	Remarks
ADD Rj, Ri	A	A6	1	CCCC	$Ri + Rj \rightarrow Ri$	
* ADD #s5, Ri	C	A4	1	CCCC	$Ri + s5 \rightarrow Ri$	
,	,	,	,	,	,	
,	,	,	,	,	,	
↓	↓	↓	↓	↓	↓	
(1)	(2)	(3)	(4)	(5)	(6)	(7)

(1) Names of instructions.

Instructions marked with * are not included in CPU specifications. These are extended instruction codes added/extended at assembly language levels.

(2) Addressing modes specified as operands are listed in symbols.
Refer to "2. Addressing mode symbols" for further information.

(3) Instruction types.

(4) Hexa-decimal expressions of instructions.

(5) Number of machine cycles needed for execution.

a: Memory access cycle. May be extended by Ready function.

b: Memory access cycle. May be extended by Ready function.

If an object register in a LD operation is referenced by an immediately following instruction, the interlock function is activated and number of cycles needed for execution increases.

c: If an immediately following instruction operates to an object of R15, SSP or USP in read/write mode or if the instruction belongs to instruction format A group, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

d: If an immediately following instruction refers to MDH/MDL, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

For a, b, c and d, minimum execution cycle is 1.

(6) Change in flag sign.

- Flag meanings
 - N : Negative flag
 - Z : Zero flag
 - V : Over flag
 - C : Carry flag
- Flag change
 - C : Change
 - : No change
 - 0 : Clear
 - 1 : Set

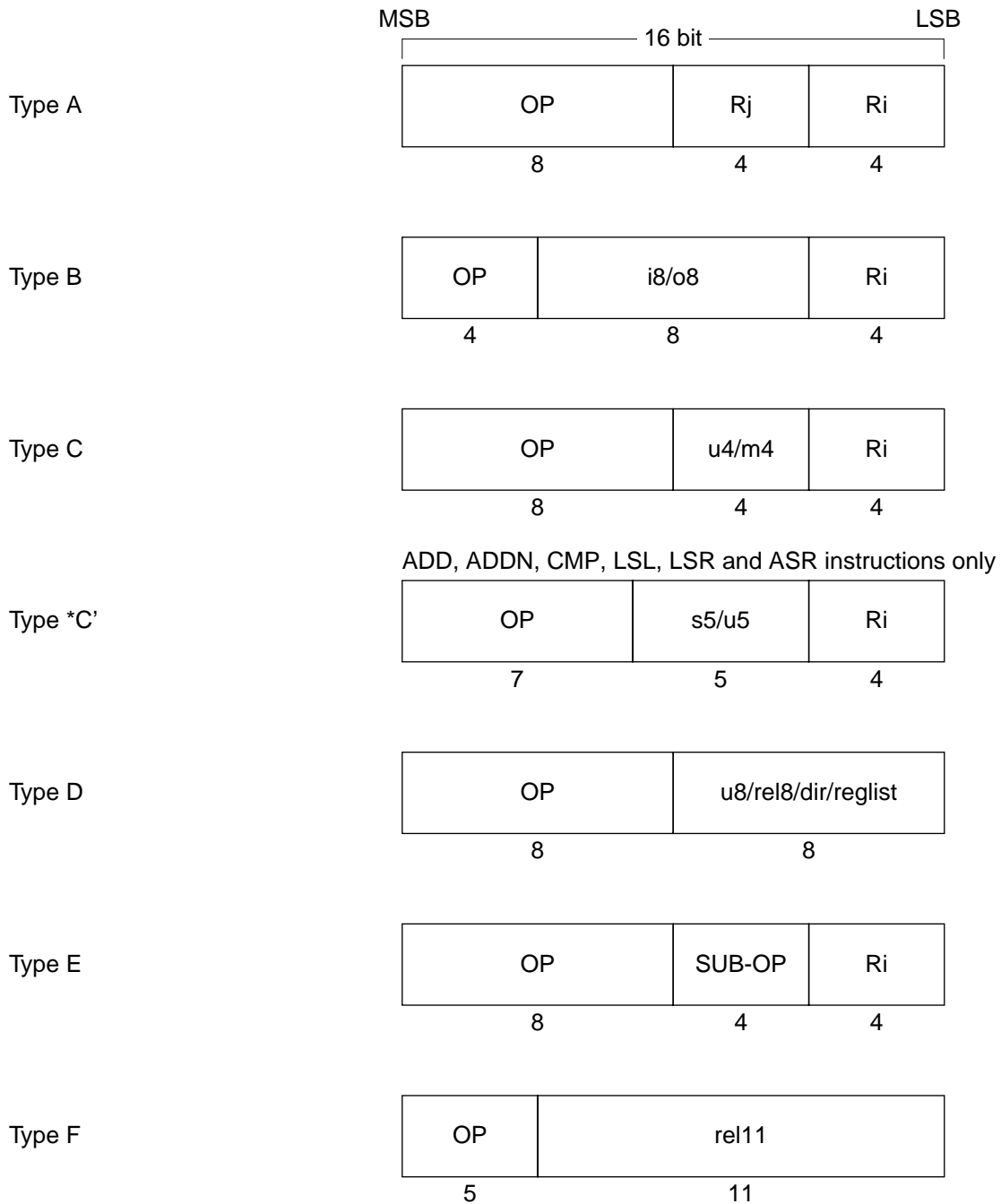
(7) Operation carried out by instruction.

2. Addressing Mode Symbols

Ri	: Register direct (R0 to R15, AC, FP, SP)
Rj	: Register direct (R0 to R15, AC, FP, SP)
R13	: Register direct (R13, AC)
Ps	: Register direct (Program status register)
Rs	: Register direct (TBR, RP, SSP, USP, MDH, MDL)
CRi	: Register direct (CR0 to CR15)
CRj	: Register direct (CR0 to CR15)
#i8	: Unsigned 8-bit immediate (–128 to 255) Note: –128 to –1 are interpreted as 128 to 255
#i20	: Unsigned 20-bit immediate (–0X80000 to 0XFFFFFF) Note: –0X7FFFF to –1 are interpreted as 0X7FFFF to 0XFFFFFF
#i32	: Unsigned 32-bit immediate (–0X80000000 to 0xFFFFFFFF) Note: –0X80000000 to –1 are interpreted as 0X80000000 to 0xFFFFFFFF
#s5	: Signed 5-bit immediate (–16 to 15)
#s10	: Signed 10-bit immediate (–512 to 508, multiple of 4 only)
#u4	: Unsigned 4-bit immediate (0 to 15)
#u5	: Unsigned 5-bit immediate (0 to 31)
#u8	: Unsigned 8-bit immediate (0 to 255)
#u10	: Unsigned 10-bit immediate (0 to 1020, multiple of 4 only)
@dir8	: Unsigned 8-bit direct address (0 to 0XFF)
@dir9	: Unsigned 9-bit direct address (0 to 0X1FE, multiple of 2 only)
@dir10	: Unsigned 10-bit direct address (0 to 0X3FC, multiple of 4 only)
label9	: Signed 9-bit branch address (–0X100 to 0XFC, multiple of 2 only)
label12	: Signed 12-bit branch address (–0X800 to 0X7FC, multiple of 2 only)
label20	: Signed 20-bit branch address (–0X80000 to 0X7FFFF)
label32	: Signed 32-bit branch address (–0X80000000 to 0X7FFFFFFF)
@Ri	: Register indirect (R0 to R15, AC, FP, SP)
@Rj	: Register indirect (R0 to R15, AC, FP, SP)
@(R13, Rj)	: Register relative indirect (Rj: R0 to R15, AC, FP, SP)
@(R14, disp10)	: Register relative indirect (disp10: –0X200 to 0X1FC, multiple of 4 only)
@(R14, disp9)	: Register relative indirect (disp9: –0X100 to 0XFE, multiple of 2 only)
@(R14, disp8)	: Register relative indirect (disp8: –0X80 to 0X7F)
@(R15, udisp6)	: Register relative (udisp6: 0 to 60, multiple of 4 only)
@Ri+	: Register indirect with post-increment (R0 to R15, AC, FP, SP)
@R13+	: Register indirect with post-increment (R13, AC)
@SP+	: Stack pop
@–SP	: Stack push
(reglist)	: Register list

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3. Instruction Types



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4. Detailed Description of Instructions

• Add/subtract operation instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ADD	Rj, Ri	A	A6	1	C C C C	$Ri + Rj \rightarrow Ri$	MSB is interpreted as a sign in assembly language
* ADD	#s5, Ri	C'	A4	1	C C C C	$Ri + s5 \rightarrow Ri$	
ADD	#u4, Ri	C	A4	1	C C C C	$Ri + \text{extu}(i4) \rightarrow Ri$	Zero-extension
ADD2	#u4, Ri	C	A5	1	C C C C	$Ri + \text{extu}(i4) \rightarrow Ri$	Sign-extension
ADDC	Rj, Ri	A	A7	1	C C C C	$Ri + Rj + c \rightarrow Ri$	Add operation with sign
ADDN	Rj, Ri	A	A2	1	- - - -	$Ri + Rj \rightarrow Ri$	MSB is interpreted as a sign in assembly language
* ADDN	#s5, Ri	C'	A0	1	- - - -	$Ri + s5 \rightarrow Ri$	
ADDN	#u4, Ri	C	A0	1	- - - -	$Ri + \text{extu}(i4) \rightarrow Ri$	Zero-extension
ADDN2	#u4, Ri	C	A1	1	- - - -	$Ri + \text{extu}(i4) \rightarrow Ri$	Sign-extension
SUB	Rj, Ri	A	AC	1	C C C C	$Ri - Rj \rightarrow Ri$	
SUBC	Rj, Ri	A	AD	1	C C C C	$Ri - Rj - c \rightarrow Ri$	Subtract operation with carry
SUBN	Rj, Ri	A	AE	1	- - - -	$Ri - Rj \rightarrow Ri$	

• Compare operation instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
CMP	Rj, Ri	A	AA	1	C C C C	$Ri - Rj$	MSB is interpreted as a sign in assembly language
* CMP	#s5, Ri	C'	A8	1	C C C C	$Ri - s5$	
CMP	#u4, Ri	C	A8	1	C C C C	$Ri + \text{extu}(i4)$	Zero-extension
CMP2	#u4, Ri	C	A9	1	C C C C	$Ri + \text{extu}(i4)$	Sign-extension

• Logical operation instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
AND	Rj, Ri	A	82	1	C C - -	$Ri \& = Rj$	Word
AND	Rj, @Ri	A	84	1+2a	C C - -	$(Ri) \& = Rj$	Word
ANDH	Rj, @Ri	A	85	1+2a	C C - -	$(Ri) \& = Rj$	Half word
ANDB	Rj, @Ri	A	86	1+2a	C C - -	$(Ri) \& = Rj$	Byte
OR	Rj, Ri	A	92	1	C C - -	$Ri = Rj$	Word
OR	Rj, @Ri	A	94	1+2a	C C - -	$(Ri) = Rj$	Word
ORH	Rj, @Ri	A	95	1+2a	C C - -	$(Ri) = Rj$	Half word
ORB	Rj, @Ri	A	96	1+2a	C C - -	$(Ri) = Rj$	Byte
EOR	Rj, Ri	A	9A	1	C C - -	$Ri \wedge = Rj$	Word
EOR	Rj, @Ri	A	9C	1+2a	C C - -	$(Ri) \wedge = Rj$	Word
EORH	Rj, @Ri	A	9D	1+2a	C C - -	$(Ri) \wedge = Rj$	Half word
EORB	Rj, @Ri	A	9E	1+2a	C C - -	$(Ri) \wedge = Rj$	Byte

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• Bit manipulation instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
BANDL	#u4, @Ri	C	80	1+2a	----	(Ri) & = (0xF0 + u4)	Manipulate lower 4 bits
BANDH	#u4, @Ri	C	81	1+2a	----	(Ri) & = ((u4 < 4) + 0x0F)	Manipulate upper 4 bits
* BAND	#u8, @Ri	*1				(Ri) & = u8	
BORL	#u4, @Ri	C	90	1+2a	----	(Ri) = u4	Manipulate lower 4 bits
BORH	#u4, @Ri	C	91	1+2a	----	(Ri) = (u4 < 4)	Manipulate upper 4 bits
* BOR	#u8, @Ri	*2			----	(Ri) = u8	
BEORL	#u4, @Ri	C	98	1+2a	----	(Ri) ^ = u4	Manipulate lower 4 bits
BEORH	#u4, @Ri	C	99	1+2a	----	(Ri) ^ = (u4 < 4)	Manipulate upper 4 bits
* BEOR	#u8, @Ri	*3			----	(Ri) ^ = u8	
BTSTL	#u4, @Ri	C	88	2+a	0 C --	(Ri) & u4	Test lower 4 bits
BTSTH	#u4, @Ri	C	89	2+a	C C --	(Ri) & (u4 < 4)	Test upper 4 bits

*1: Assembler generates BANDL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BANDH if “u8&0xF0” leaves an active bit. Depending on the value in the “u8” format, both BANDL and BANDH may be generated.

*2: Assembler generates BORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BORH if “u8&0xF0” leaves an active bit.

*3: Assembler generates BEORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BEORH if “u8&0xF0” leaves an active bit.

• Add/subtract operation instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MUL	Rj, Ri	A	AF	5	C C C -	Ri * Rj → MDH, MDL	32-bit*32-bit = 64-bit
MULU	Rj, Ri	A	AB	5	C C C -	Ri * Rj → MDH, MDL	Unsigned
MULH	Rj, Ri	A	BF	3	C C --	Ri * Rj → MDL	16-bit*16-bit = 32-bit
MULUH	Rj, Ri	A	BB	3	C C --	Ri * Rj → MDL	Unsigned
DIVOS	Ri	E	97-4	1	----		Step calculation
DIVOU	Ri	E	97-5	1	----		32-bit/32-bit = 32-bit
DIV1	Ri	E	97-6	d	- C - C		
DIV2	Ri	E	97-7	1	- C - C		
DIV3	Ri	E	9F-6	1	----		
DIV4S	Ri	E	9F-7	1	----		
* DIV	Ri	*1		36	- C - C	MDL/Ri → MDL, MDL%Ri → MDH	
* DIVU	Ri	*2		33	- C - C	MDL/Ri → MDL, MDL%Ri → MDH	

*1: DIVOS, DIV1 × 32, DIV2, DIV3 and DIV4S are generated. A total instruction code length of 72 bytes.

*2: DIVOU and DIV1 × 32 are generated. A total instruction code length of 66 bytes.

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• Shift instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LSL	Rj, Ri	A	B6	1	C C - C	Ri << Rj → Ri	Logical shift
* LSL	#u5, Ri (u5: 0 ~ 31)	C'	B4	1	C C - C	Ri << u5 → Ri	
LSL	#u4, Ri	C	B4	1	C C - C	Ri << u4 → Ri	
* LSL2	#u4, Ri	C	B5	1	C C - C	Ri << (u4 + 16) → Ri	
LSR	Rj, Ri	A	B2	1	C C - C	Ri >> Rj → Ri	Logical shift
* LSR	#u5, Ri (u5: 0 ~ 31)	C'	B0	1	C C - C	Ri >> u5 → Ri	
LSR	#u4, Ri	C	B0	1	C C - C	Ri >> u4 → Ri	
* LSR2	#u4, Ri	C	B1	1	C C - C	Ri >> (u4 + 16) → Ri	
ASR	Rj, Ri	A	BA	1	C C - C	Ri >> Rj → Ri	Logical shift
* ASR	#u5, Ri (u5: 0 ~ 31)	C'	B8	1	C C - C	Ri >> u5 → Ri	
ASR	#u4, Ri	C	B8	1	C C - C	Ri >> u4 → Ri	
* ASR2	#u4, Ri	C	B9	1	C C - C	Ri >> (u4 + 16) → Ri	

• Immediate value set/16-bit/32-bit immediate value transfer instruction

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LDI:32	#i32, Ri	E	9F-8	3	- - - -	i32 → Ri	Upper 12-bit is zero-extended Upper 24-bit is zero-extended
LDI:20	#i20, Ri	C	9B	2	- - - -	i20 → Ri	
LDI:8	#i8, Ri	B	C0	1	- - - -	i8 → Ri	
* LDI	# {i8 i20 i32}, Ri					{i8 i20 i32} → Ri	

* : If an immediate value is given in absolute, assembler automatically makes i8, i20 or i32 selection.
If an immediate value contains relative value or external reference, assembler selects i32.

• Memory load instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LD	@Rj, Ri	A	04	b	- - - -	(Rj) → Ri	Rs: Special register *
LD	@(R13, Rj), Ri	A	00	b	- - - -	(R13 + Rj) → Ri	
LD	@(R14, disp10), Ri	B	20	b	- - - -	(R14 + disp10) → Ri	
LD	@(R15, udisp6), Ri	C	03	b	- - - -	(R15 + udisp6) → Ri	
LD	@R15 +, Ri	E	07-0	b	- - - -	(R15) → Ri, R15 += 4	
LD	@R15 +, Rs	E	07-8	b	- - - -	(R15) → Rs, R15 += 4	
LD	@R15 +, PS	E	07-9	1+a+b	C C C C	(R15) → PS, R15 += 4	
LDUH	@Rj, Ri	A	05	b	- - - -	(Rj) → Ri	Zero-extension
LDUH	@(R13, Rj), Ri	A	01	b	- - - -	(R13 + Rj) → Ri	
LDUH	@(R14, disp9), Ri	B	40	b	- - - -	(R14 + disp9) → Ri	
LDUB	@Rj, Ri	A	06	b	- - - -	(Rj) → Ri	Zero-extension
LDUB	@(R13, Rj), Ri	A	02	b	- - - -	(R13 + Rj) → Ri	
LDUB	@(R14, disp8), Ri	B	60	b	- - - -	(R14 + disp8) → Ri	

* : Assembler calculates and set the result in the field of o8, o4 format given by hardware specification.
disp10/4 → o8, disp9/2 → o8, disp8 → o8, disp10, disp9, disp8 are signed
udisp6/4 → o4, udisp6 are unsigned.

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• Memory store instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ST	Ri, @Rj	A	14	a	----	Ri → (Rj)	Word
ST	Ri, @(R13, Rj)	A	10	a	----	Ri → (R13 + Rj)	Word
ST	Ri, @(R14, disp10)	B	30	a	----	Ri → (R14 + disp10)	Word
ST	Ri, @(R15, udisp6)	C	13	a	----	Ri → (R15 + udisp6)	
ST	Ri, @-R15	E	17-0	a	----	R15 -= 4, Ri → (R15)	
ST	Rs, @-R15	E	17-8	a	----	R15 -= 4, Rs → (R15)	Rs: Special register
ST	PS, @-R15	E	17-9	a	----	R15 -= 4, PS → (R15)	*
STH	Ri, @Rj	A	15	a	----	Ri → (Rj)	Half word
STH	Ri, @(R13, Rj)	A	11	a	----	Ri → (R13 + Rj)	Half word
STH	Ri, @(R14, disp9)	B	50	a	----	Ri → (R14 + disp9)	Half word
STB	Ri, @Rj	A	16	a	----	Ri → (Rj)	Byte
STB	Ri, @(R13, Rj)	A	12	a	----	Ri → (R13 + Rj)	Byte
STB	Ri, @(R14, disp8)	B	70	a	----	Ri → (R14 + disp8)	Byte

* : Assembler calculates and set the result in the field of o8, o4 format given by hardware specification.
 disp10/4 → o8, disp9/2 → o8, disp8 → o8, disp10, disp9, disp8 are signed
 udisp6/4 → o4, udisp6 are unsigned.

• Transfer instructions between registers

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MOV	Rj, Ri	A	8B	1	----	Rj → Ri	Transfer between general-purpose registers
MOV	Rs, Ri	A	B7	1	----	Rs → Ri	Rs: Special register
MOV	Ri, Rs	A	B3	1	----	Ri → Rs	Rs: Special register
MOV	PS, Ri	E	17-1	1	----	PS → Ri	*
MOV	Ri, PS	E	07-1	c	CCCC	Ri → PS	

* : Special registers Rs: TBR, RP USP, SSP, MDH, MDL

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• Normal branch (non-delay) instructions

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP	@Ri	E	97-0	2	- - - -	Ri → PC	
CALL	label12	F	D0	2	- - - -	PC + 2 → RP, PC + 2 + (label12 - PC - 2) → PC	
CALL	@Ri	E	97-1	2	- - - -	PC + 2 → RP, Ri → PC	
RET		E	97-2	2	- - - -	RP → PC	Return
INT	#u8	D	1F	3+3a	- - - -	SSP - = 4, PS → (SSP), SSP - = 4, PC + 2 → (SSP), 0 → I flag, 0 → S flag, (TBR + 0x3FC - u8 × 4) → PC	For emulator
INTE		E	9F-3	3+3a	- - - -	SSP - = 4, PS → (SSP), SSP - = 4, PC + 2 → (SSP), 0 → S flag, (TBR + 0x3D8) → PC	
RETI		E	97-3	2+2a	C C C C	(R15) → PC, R15 - = 4, (R15) → PS, R15 - = 4	
BRA	label9	D	E0	2	- - - -	PC + 2 + (label9 - PC - 2) → PC	
BNO	label9	D	E1	1	- - - -	Non-branch	
BEQ	label9	D	E2	2/1	- - - -	if (Z == 1) then PC + 2 + (label9 - PC - 2) → PC	
BNE	label9	D	E3	2/1	- - - -	PCx/Z == 0	
BC	label9	D	E4	2/1	- - - -	PCs/C == 1	
BNC	label9	D	E5	2/1	- - - -	PCs/C == 0	
BN	label9	D	E6	2/1	- - - -	PCs/N == 1	
BP	label9	D	E7	2/1	- - - -	PCs/N == 0	
BV	label9	D	E8	2/1	- - - -	PCs/V == 1	
BNV	label9	D	E9	2/1	- - - -	PCs/V == 0	
BLT	label9	D	EA	2/1	- - - -	PCs/V xor N == 1	
BGE	label9	D	EB	2/1	- - - -	PCs/V xor N == 0	
BLE	label9	D	EC	2/1	- - - -	PCs/(V xor N) or Z == 1	
BGT	label9	D	ED	2/1	- - - -	PCs/(V xor N) or Z == 0	
BLS	label9	D	EE	2/1	- - - -	PCs/C or Z == 1	
BHI	label9	D	EF	2/1	- - - -	PCs/C or Z == 0	

- Notes:
- Number of cycles "2/1" indicates that 2 cycles are needed for branch and 1 cycle needed for non-branch.
 - Assembler calculates and set the result in the field of rel11 and rel8 format given by hardware specification. (label12 - PC - 2)/2 → rel11, (label9 - PC - 2)/2 → rel8, label12, label9 are signed.
 - RETI must be operated while S flag = 0.

MB91103 Series

• Branch instructions with delays

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
JMP:D @Ri	E	9F-0	1	- - - -	Ri → PC	
CALL:D label12	F	D8	1	- - - -	PC + 4 → RP, PC + 2 + (label12 - PC - 2) → PC	
CALL:D @Ri	E	9F-1	1	- - - -	PC + 4 → RP, Ri → PC	
RET:D	E	9F-2	1	- - - -	RP → PC	Return
BRA:D label9	D	F0	1	- - - -	PC + 2 + (label9 - PC - 2) → PC	
BNO:D label9	D	F1	1	- - - -	Non-branch	
BEQ:D label9	D	F2	1	- - - -	if (Z == 1) then PC + 2 + (label9 - PC - 2) → PC	
BNE:D label9	D	F3	1	- - - -	PCs/Z == 0	
BC:D label9	D	F4	1	- - - -	PCs/C == 1	
BNC:D label9	D	F5	1	- - - -	PCs/C == 0	
BN:D label9	D	F6	1	- - - -	PCs/N == 1	
BP:D label9	D	F7	1	- - - -	PCs/N == 0	
BV:D label9	D	F8	1	- - - -	PCs/V == 1	
BNV:D label9	D	F9	1	- - - -	PCs/V == 0	
BLT:D label9	D	FA	1	- - - -	PCs/V xor N == 1	
BGE:D label9	D	FB	1	- - - -	PCs/V xor N == 0	
BLE:D label9	D	FC	1	- - - -	PCs/(V xor N) or Z == 1	
BGT:D label9	D	FD	1	- - - -	PCs/(V xor N) or Z == 0	
BLS:D label9	D	FE	1	- - - -	PCs/C or Z == 1	
BHI:D label9	D	FF	1	- - - -	PCs/C or Z == 0	

- Notes:
- Assembler calculates and set the result in the field of rel11 and rel8 format given by hardware specification. (label12 - PC - 2)/2 → rel11, (label9 - PC - 2)/2 → rel8, label12, label9 are signed.
 - Delayed branch operation always executes next instruction (delay slot) before making a branch.
 - Instructions allowed to be stored in the delay slot are all 1-cycle, a, b, c and d-cycle instructions. Multiple-cycle instructions are no to allowed on the delay slot.

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• Others

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
NOP	E	9F-A	1	- - - -	No changes	
ANDCCR #u8	D	83	c	C C C C	CCR and u8 → CCR	
ORCCR #u8	D	93	c	C C C C	CCR or u8 → CCR	
STILM #u8	D	87	1	- - - -	i8 → ILM	Set ILM immediate value
ADDSP #s10	D	A3	1	- - - -	R15 + = s10	ADD SP instruction
	*1					
EXTSB Ri	E	97-8	1	- - - -	Sign extension 8 → 32-bit	
EXTUB Ri	E	97-9	1	- - - -	Zero extension 8 → 32-bit	
EXTSH Ri	E	97-A	1	- - - -	Sign extension 16 → 32 bit	
EXTUH Ri	E	97-B	1	- - - -	Zero extension 16 → 32-bit	
LDM0 (reglist)	D	8C		- - - -	(R15) → reglist, R15 increment	Load-multi R0 to R7
LDM1 (reglist)	D	8D		- - - -	(R15) → reglist, R15 increment	Load-multi R8 to R15
* LDM (reglist)				- - - -	(R15) → reglist, R15 increment	Load-multi R0 to R15
	*2					
STM0 (reglist)	D	8E		- - - -	R15 decrement, reglist → (R15)	Store-multi R0 to R7
STM1 (reglist)	D	8F		- - - -	R15 decrement, reglist → (R15)	Store-multi R8 to R15
* STM2 (reglist)				- - - -	R15 decrement, reglist → (R15)	Store-multi R0 to R15
	*3					
ENTER #u10	D	0F	1+a	- - - -	R14 → (R15 - 4), R15 - 4 → R14, R15 - u10 → R15	Entrance processing of function
	*4					
LEAVE	E	9F-9	b	- - - -	R14 + 4 → R15, (R15 - 4) → R14	Exit processing of function
XCHB @Rj, Ri	A	8A	2a	- - - -	Rj → TEMP (Rj) → Ri TEMP → (Rj)	For SEMAFO management Byte data

*1: For s10 format, assembler calculates s10/4 and convert to s8 format. s10 is signed.

*2: If either of R0 to R7 is specified in reglist, assembler generates LDM0. If either of R8 to R15 is specified, assembler generates LDM1. Both LDM0 and LDM1 may be generated.

*3: If either of R0 to R7 is specified in reglist, assembler generates STM0. If either of R8 to R15 is specified, assembler generates STM1. Both STM0 and STM1 may be generated.

*4: For u10 format, assembler calculates u10/4 and convert to s8 format. u10 is unsigned.

Notes: • Number of cycles needed for execution of LDM0 (reglist) and LDM1 (reglist) is given by the following calculation;

$a*(n - 1) + b + 1$ where n is number of registers specified.

• Number of cycles needed for execution of STM0 (reglist) and STM1 (reglist) is given by the following calculation;

$a*n + 1$ where n is number of registers specified.

MB91103 Series

• 20-bit normal branch macro instructions

Mnemonic		Operation	Remarks
* CALL20	label20, Ri	Next instruction address → RP, label20 → PC	Ri: Temporary register *1
* BRA20	label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20	label20, Ri	if (Z == 1) then label20 → PC	Ri: Temporary register *3
* BNE20	label20, Ri	ifs/Z == 0	Ri: Temporary register *3
* BC20	label20, Ri	ifs/C == 1	Ri: Temporary register *3
* BNC20	label20, Ri	ifs/C == 0	Ri: Temporary register *3
* BN20	label20, Ri	ifs/N == 1	Ri: Temporary register *3
* BP20	label20, Ri	ifs/N == 0	Ri: Temporary register *3
* BV20	label20, Ri	ifs/V == 1	Ri: Temporary register *3
* BNV20	label20, Ri	ifs/V == 0	Ri: Temporary register *3
* BLT20	label20, Ri	ifs/V xor N == 1	Ri: Temporary register *3
* BGE20	label20, Ri	ifs/V xor N == 0	Ri: Temporary register *3
* BLE20	label20, Ri	ifs/(V xor N) or Z == 1	Ri: Temporary register *3
* BGT20	label20, Ri	ifs/(V xor N) or Z == 0	Ri: Temporary register *3
* BLS20	label20, Ri	ifs/C or Z == 1	Ri: Temporary register *3
* BHI20	label20, Ri	ifs/C or Z == 0	Ri: Temporary register *3

*1: CALL20

- If label20-PC-2 is between -0x800 and +0x7fe, instruction is generated as follows;
CALL label12
- If label20-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:20 #label20, Ri
CALL @Ri

*2: BRA20

- If label20-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
BRA label9
- If label20-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:20 #label20, Ri
JMP @Ri

*3: Bcc20 (BEQ20 to BHI20)

- If label20-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
Bcc label9
- If label20-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
Bxcc false xcc is a revolt condition of cc
LDI:20 #label20, Ri
JMP @Ri
false:

MB91103 Series

• 20-bit delayed branch macro instructions

Mnemonic	Operation	Remarks
* CALL20:D label20, Ri	Next instruction address + 2 → RP, label20 → PC	Ri: Temporary register *1
* BRA20:D label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20:D label20, Ri	if (Z == 1) then label20 → PC	Ri: Temporary register *3
* BNE20:D label20, Ri	ifs/Z == 0	Ri: Temporary register *3
* BC20:D label20, Ri	ifs/C == 1	Ri: Temporary register *3
* BNC20:D label20, Ri	ifs/C == 0	Ri: Temporary register *3
* BN20:D label20, Ri	ifs/N == 1	Ri: Temporary register *3
* BP20:D label20, Ri	ifs/N == 0	Ri: Temporary register *3
* BV20:D label20, Ri	ifs/V == 1	Ri: Temporary register *3
* BNV20:D label20, Ri	ifs/V == 0	Ri: Temporary register *3
* BLT20:D label20, Ri	ifs/V xor N == 1	Ri: Temporary register *3
* BGE20:D label20, Ri	ifs/V xor N == 0	Ri: Temporary register *3
* BLE20:D label20, Ri	ifs/(V xor N) or Z == 1	Ri: Temporary register *3
* BGT20:D label20, Ri	ifs/(V xor N) or Z == 0	Ri: Temporary register *3
* BLS20:D label20, Ri	ifs/C or Z == 1	Ri: Temporary register *3
* BHI20:D label20, Ri	ifs/C or Z == 0	Ri: Temporary register *3

*1: CALL20:D

- If label20-PC-2 is between -0x800 and +0x7fe, instruction is generated as follows;
CALL:D label12
- If label20-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:20 #label20, Ri
CALL:D @Ri

*2: BRA20:D

- If label20-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
BRA:D label9
- If label20-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:20 #label20, Ri
JMP:D @Ri

*3: Bcc20:D (BEQ20:D to BHI20:D)

- If label20-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
Bcc:D label9
- If label20-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
Bxcc false xcc is a revolt condition of cc
LDI:20 #label20, Ri
JMP:D @Ri
false:

MB91103 Series

• 32-bit normal macro branch instructions

Mnemonic		Operation	Remarks
* CALL32	label32, Ri	Next instruction address → RP, label32 → PC	Ri: Temporary register *1
* BRA32	label32, Ri	label32 → PC	Ri: Temporary register *2
* BEQ32	label32, Ri	if (Z == 1) then label32 → PC	Ri: Temporary register *3
* BNE32	label32, Ri	ifs/Z == 0	Ri: Temporary register *3
* BC32	label32, Ri	ifs/C == 1	Ri: Temporary register *3
* BNC32	label32, Ri	ifs/C == 0	Ri: Temporary register *3
* BN32	label32, Ri	ifs/N == 1	Ri: Temporary register *3
* BP32	label32, Ri	ifs/N == 0	Ri: Temporary register *3
* BV32	label32, Ri	ifs/V == 1	Ri: Temporary register *3
* BNV32	label32, Ri	ifs/V == 0	Ri: Temporary register *3
* BLT32	label32, Ri	ifs/V xor N == 1	Ri: Temporary register *3
* BGE32	label32, Ri	ifs/V xor N == 0	Ri: Temporary register *3
* BLE32	label32, Ri	ifs/(V xor N) or Z == 1	Ri: Temporary register *3
* BGT32	label32, Ri	ifs/(V xor N) or Z == 0	Ri: Temporary register *3
* BLS32	label32, Ri	ifs/C or Z == 1	Ri: Temporary register *3
* BHI32	label32, Ri	ifs/C or Z == 0	Ri: Temporary register *3

*1: CALL32

- If label32-PC-2 is between -0x800 and +0x7fe, instruction is generated as follows;
CALL label12
- If label32-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:32 #label32, Ri
CALL @Ri

*2: BRA32

- If label32-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
BRA label9
- If label32-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:32 #label32, Ri
JMP @Ri

*3: Bcc32 (BEQ32 to BHI32)

- If label32-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
Bcc label9
- If label32-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
Bxcc false xcc is a revolt condition of cc
LDI:32 #label32, Ri
JMP @Ri
false:

MB91103 Series

• 32-bit delayed macro branch instructions

Mnemonic	Operation	Remarks
* CALL32:D label32, Ri	Next instruction address + 2 → RP, label32 → PC	Ri: Temporary register *1
* BRA32:D label32, Ri	label32 → PC	Ri: Temporary register *2
* BEQ32:D label32, Ri	if (Z == 1) then label32 → PC	Ri: Temporary register *3
* BNE32:D label32, Ri	ifs/Z == 0	Ri: Temporary register *3
* BC32:D label32, Ri	ifs/C == 1	Ri: Temporary register *3
* BNC32:D label32, Ri	ifs/C == 0	Ri: Temporary register *3
* BN32:D label32, Ri	ifs/N == 1	Ri: Temporary register *3
* BP32:D label32, Ri	ifs/N == 0	Ri: Temporary register *3
* BV32:D label32, Ri	ifs/V == 1	Ri: Temporary register *3
* BNV32:D label32, Ri	ifs/V == 0	Ri: Temporary register *3
* BLT32:D label32, Ri	ifs/V xor N == 1	Ri: Temporary register *3
* BGE32:D label32, Ri	ifs/V xor N == 0	Ri: Temporary register *3
* BLE32:D label32, Ri	ifs/(V xor N) or Z == 1	Ri: Temporary register *3
* BGT32:D label32, Ri	ifs/(V xor N) or Z == 0	Ri: Temporary register *3
* BLS32:D label32, Ri	ifs/C or Z == 1	Ri: Temporary register *3
* BHI32:D label32, Ri	ifs/C or Z == 0	Ri: Temporary register *3

*1: CALL32:D

- If label32-PC-2 is between -0x800 and +0x7fe, instruction is generated as follows;
CALL:D label12
- If label32-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:32 #label32, Ri
CALL:D @Ri

*2: BRA32:D

- If label32-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
BRA:D label9
- If label32-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
LDI:32 #label32, Ri
JMP:D @Ri

*3: Bcc32:D (BEQ32:D to BHI32:D)

- If label32-PC-2 is between -0x100 and +0xfe, instruction is generated as follows;
Bcc:D label9
- If label32-PC-2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;
Bxcc false xcc is a revolt condition of cc
LDI:32 #label32, Ri
JMP:D @Ri
false:

MB91103 Series

• Direct addressing instructions

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
DMOV @dir10, R13	D	08	b	----	(dir10) → R13	Word
DMOV R13, @dir10	D	18	a	----	R13 → (dir10)	Word
DMOV @dir10, @R13+	D	0C	2a	----	(dir10) → (R13), R13 + = 4	Word
DMOV @R13+, @dir10	D	1C	2a	----	(R13) → (dir10), R13 + = 4	Word
DMOV @dir10, @-R15	D	0B	2a	----	R15 - = 4, (R15) → (dir10)	Word
DMOV @R15+, @dir10	D	1B	2a	----	(R15) → (dir10), R15 + = 4	Word
DMOVH @dir9, R13	D	09	b	----	(dir9) → R13	Half word
DMOVH R13, @dir9	D	19	a	----	R13 → (dir9)	Half word
DMOVH @dir9, @R13+	D	0D	2a	----	(dir9) → (R13), R13 + = 2	Half word
DMOVH @R13+, @dir9	D	1D	2a	----	(R13) → (dir9), R13 + = 2	Half word
DMOV B @dir8, R13	D	0A	b	----	(dir8) → R13	Byte
DMOV B R13, @dir8	D	1A	a	----	R13 → (dir8)	Byte
DMOV B @dir8, @R13+	D	0E	2a	----	(dir8) → (R13), R13 + +	Byte
DMOV B @R13+, @dir8	D	1E	2a	----	(R13) → (dir8), R13 + +	Byte

Note: Assembler calculates as follows and set the result value to dir8, dir9 and dir10 fields.

dir8 → dir, dir9/2 → dir, dir10/4 → dir, dir8, dir9, dir10 are unsigned.

• Resource instructions

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
LDRES @Ri+, #u4	C	BC	a	----	(Ri) → u4 resource Ri + = 4	u4: Channel number
STRES #u4, @Ri+	C	BD	a	----	u4 resource → (Ri) Ri + = 4	u4: Channel number

• Co-processor control instructions

{CRi | CRj}: = CR0 | CR1 | CR2 | CR3 | CR4 | CR5 | CR6 | CR7 | CR8 | CR9 | CR10 | CR11 | CR12 | CR13 | CR14 | CR15

u4: Specify channel

u8: Specify command

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
COPOP #u4, #u8, CRj, CRi	E	9F-C	2+a	----	Calculation	
COPLD #u4, #u8, Rj, CRi	E	9F-D	1+2a	----	Rj → CRi	
COPST #u4, #u8, CRj, Ri	E	9F-E	1+2a	----	CRj → Ri	
COPSV #u4, #u8, CRj, Ri	E	9F-F	1+2a	----	CRj → Ri	No error traps

Note: These instructions are not valid because this model does not have a co-processor.

MB91103 Series

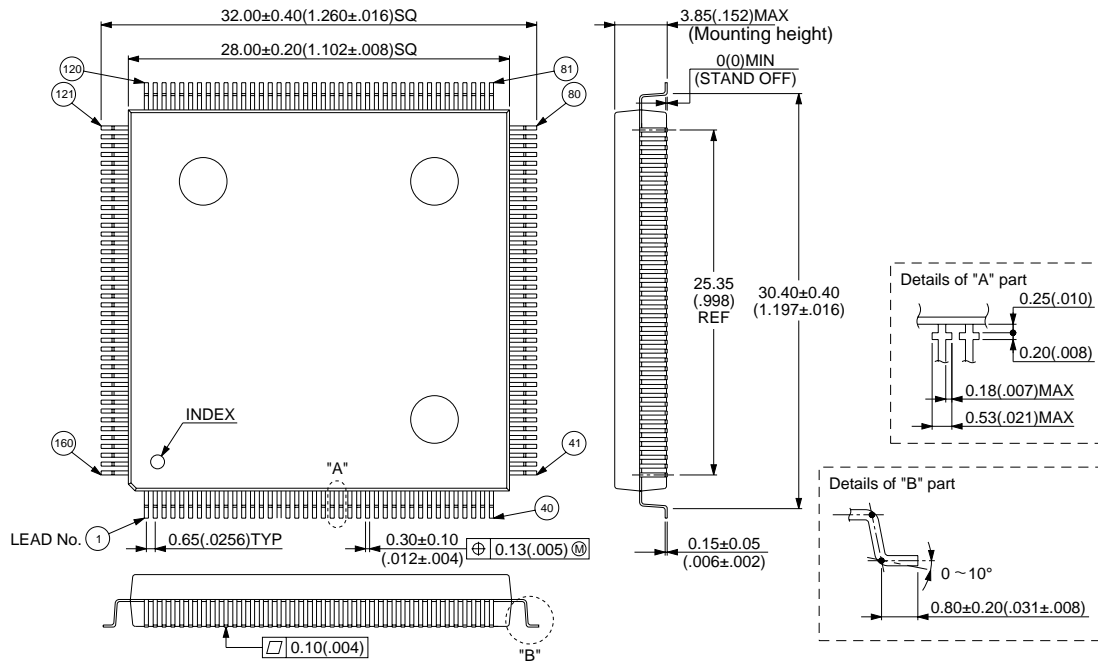
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91103	160-pin Plastic QFP FPT-160P-M03	

MB91103 Series

■ PACKAGE DIMENSIONS

160-pin Plastic QFP
(FPT-160P-M03)



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Dimensions in mm (inches)

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